Micro-Coaxial Lines for Active Hybrid-Monolithic Circuits

Negar Ehsan[1], Evan Cullens[1], Kenneth Vanhille[2], Dave Frey[3],
Sébastien Rondineau[4], Robert Actis[5], Sue Jessup[5], Robert Lender Jr.[5],
Anthony Immorlica[5], Deepukumar Nair[6], Dejan Filipović[1], Zoya Popović[1]

[1]Department of Electrical and Computer Engineering, University of Colorado, Boulder, CO 80309, USA
[2]Nuvotronics LLC, Blacksburg, VA 24060, USA
[3]Cobham Defense Electronic Systems, Lansdale, PA 19446, USA
[4]TSM Antennas, Rodovia RST 287, 9900 Camobi, Santa Maria, RS 97105-030, Brazil
[5]BAE Systems, Nashua, NH 03061, USA
[6]DuPont Electronic Technologies, Research Triangle Park, NC 27709, USA

***Abstract*— This paper discusses fundamental properties of rectangular micro-coaxial lines fabricated in the PolyStrata™ process for broadband applications from 2–20 GHz. The possible impedance ranges for coaxial lines implemented with both five and eleven Cu layers are discussed and compared with measured results for the lowest impedance (8 Ω) line. Power handling and thermal properties of these miniature lines are analyzed and measured. A 50 Ω line with outer conductor cross-section of 600μm by 400μm is experimentally shown to handle 53 W at 2.5 GHz with a 10 % duty cycle. Integration with active components is investigated and a 1–10 GHz measurement of a GaN 50 Ω MMIC amplifier shows minimal performance degradation relative to on-wafer measurements.**

I. Introduction

Millimeter-wave components implemented with rectangular micro-coaxial lines have been demonstrated in the PolyStrata™ [1] and EFAB™ [2] processes, with passive devices such as couplers [3], [4], antennas [5], resonators [6], and filters [7]. This paper addresses fundamental properties of micro-coaxial lines for microwave broadband hybrid-monolithic integration with active devices. In order to design, e.g., a broadband solid state power amplifier, matching circuits might require a broad range of characteristic impedances that can handle tens of watts of power with low loss.

A section of a 50 Ω rectangular micro-coaxial line is shown in Fig. 1 with its physical dimensions indicated. The Cu inner conductor is supported in air by periodic dielectric support straps. The outer conductor contains release holes that serve to drain the photoresist in the last step of the fabrication. The rf designs are constrained by fabrication requirements, which include the number of Cu layers that comprise the coaxial line, dielectric support thermal properties, aspect ratio and thickness of Cu layers and air gaps, position of release holes [8], and wafer/circuit layout for footprint reduction. In addition, incorporating active devices into a coaxial environment poses issues related to both monolithic and hybrid integration techniques, and the interconnects and assembly structures become a core component of the monolithic PolyStrata™ design.

This paper is organized as follows:

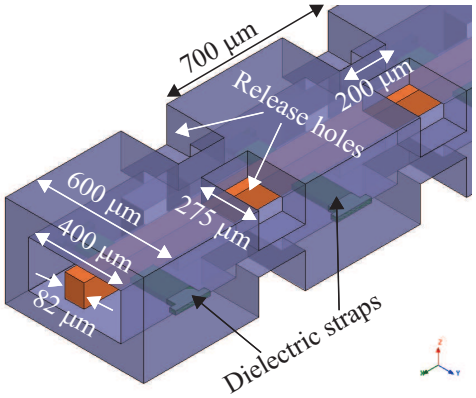

Fig. 1. Physical geometry of a 50 Ω rectangular micro-coaxial line. The inner conductor is supported in air by periodic dielectric support straps that take up a very small percentage of the total volume, resulting in very low loss [9]. The outer conductor contains holes that serve to drain the photoresist in the last fabrication step. The aspect ratio and relative dimensions of the inner and outer conductor determine the characteristic impedance.

- In Section II, the profile of five-layer and eleven-layer lines is given, along with a discussion of possible characteristic impedance values given the fabrication constraints. Validation with experiment is presented for an 8 Ω line.
- Section III discusses the CW and pulsed power handling capability of the micro-coaxial lines along with thermal and breakdown simulations.
- Section IV shows a possible way of hybrid-monolithic integration with active devices in the example of a 1–10 GHz flip-chip mounted MMIC GaN amplifier. The design of an interconnect and assembly component, referred to as an "active socket" is presented. The amplifier gain was measured on-wafer using a standard probe station setup and compared to the gain when the amplifier chip is integrated into the micro-coaxial environment.

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II. Characteristic Impedances Available with Micro-Coaxial Lines

The PolyStrata™ process is a sequential deposition fabrication process with Cu layers that each can vary from 10 µm–100 µm in thickness. Increasing the number of layers provides additional design flexibility, but fabrication time is directly proportional to the number of layers. This paper discusses both a five-layer process that is fast and reliable, and an eleven-layer process that allows for higher power levels and more design flexibility, with cross-sections shown in Fig. 2. The available characteristic impedances versus inner conductor widths of the two configurations are calculated using the method from [9] and are shown in Fig. 3. The design variables b_{11} and b_5 indicate the heights of the inner conductors for the eleven-layer and the five-layer lines, respectively. The inner width of the outer conductor W_a in Fig. 2 (b) is 1350 µm wide for the traces labeled b_{11}, and the inner width of the outer conductor W_a in Fig. 2 (a) is 1200 µm for the trace labeled b_5.

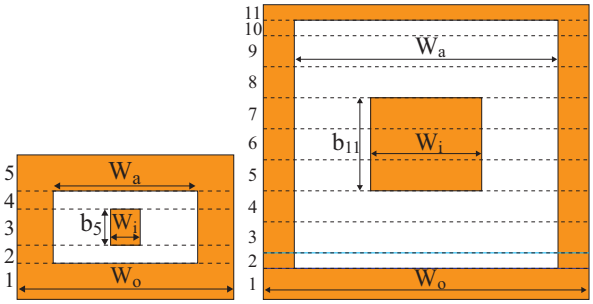


Fig. 2. (a) Cross-section of the five-layer micro-coaxial line. The height of layers 1, 3, and 5 is 100 µm, and layers 2 and 4 are 50 µm tall. (b) Cross-section of the eleven-layer micro-coaxial line; the height of layers 2, 10, and 11 is 50 µm; all other layers are 100 µm tall.

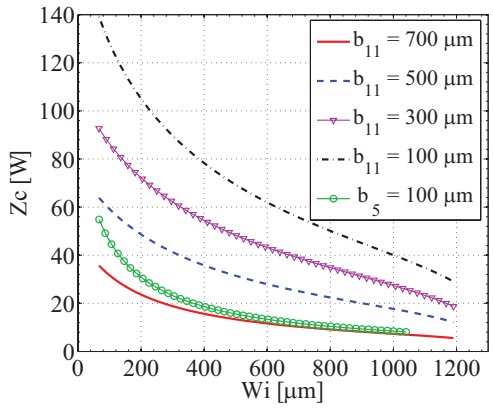


Fig. 3. Possible characteristic impedances for the eleven-layer and five-layer micro-coaxial lines versus inner conductor widths of the eleven-layer and five-layer lines. Variables b_{11} and b_5 indicate the height of the inner conductor for the eleven-layer and five-layer lines, respectively. The traces labeled b_{11} correspond to $W_a = 1350$ µm, and the traces labeled b_5 are for $W_a = 1200$ µm.

The eleven-layer line enables greater design flexibility since the inner conductor can be fabricated with between one and seven layers, for a total height from 100 µm to 700 µm. The resulting dimensions correspond to characteristic impedances from 6 Ω to 140 Ω. The impedance range for a five-layer line with dimensions shown in Fig. 2 (a) with a single-layer inner conductor is 8 Ω–55 Ω.

In order to confirm the characteristic impedances of the rectangular coaxial lines shown in Fig. 3, an 8 Ω line ($W_i = 960$ µm, and $W_a = 1200$ µm) was implemented in the five-layer process. Fig. 4 (a) shows the simulated vs. measured S-parameter results of the 8 Ω line terminated in 50 Ω input and output ports. This line was analyzed with Ansoft High Frequency Structure Simulator (HFSS™), a full-wave FEM simulation tool. The measurement was performed using an HP8510C network analyzer with a probe station. The calibration was performed with an on-wafer TRL calibration standard set with two line lengths for the required bandwidth. Fig. 4 (b) and (c) show the low- and high-frequency line measurements from 2 to 20 GHz. The lengths of the two lines are 16.8 mm and 4.9 mm, respectively.

III. Power Handling

For biasing active components, it is critical to determine the minimum cross-section of the inner conductor that can handle the required dc current. Ohmic loss calculations show that 2.5 A of dc current necessitates an inner conductor cross-section ≥ 65 µm^2, so the 100 µm minimum height shown in Fig. 2 includes a reasonable margin of safety. The main limitations for both dc and rf power handling are the 200 °C glass-transition temperature of the dielectric straps, and electric field breakdown around sharp metal edges.

Static thermal simulations are performed using Ansoft ePhysics™ FEM software, assuming the temperature of the outer conductor is fixed at 25 °C and the structure is placed in an air boundary box with a fixed temperature of 25 °C. The line was first simulated at 20 GHz using HFSS™ in order to extract the conductor and dielectric losses. The plot of the temperature profile for the five-layer 50 Ω low-frequency TRL line standard is shown in Fig. 5. The line is simulated with 100 µm wide periodic dielectric support straps that are 700 µm apart, and with release holes as shown in Fig. 1. A comparison of maximum temperatures for the lines from Fig. 2 is given in Table I for both 10 W and 20 W of incident power from a matched generator. Note that these are worst-case temperatures, since there is no additional heatsinking, no radiative heat transfer is taken into account, and it is assumed that there are no thermally-conductive interconnects at the two ends of the line.

TABLE I
Static Thermal Analysis of 50 Ω Lines at 20 GHz

Line	Power [W]	Temp [°C]
Five-layer 50 Ω	10 / 20	183 / 341
Eleven-layer 50 Ω	10 / 20	72 / 120

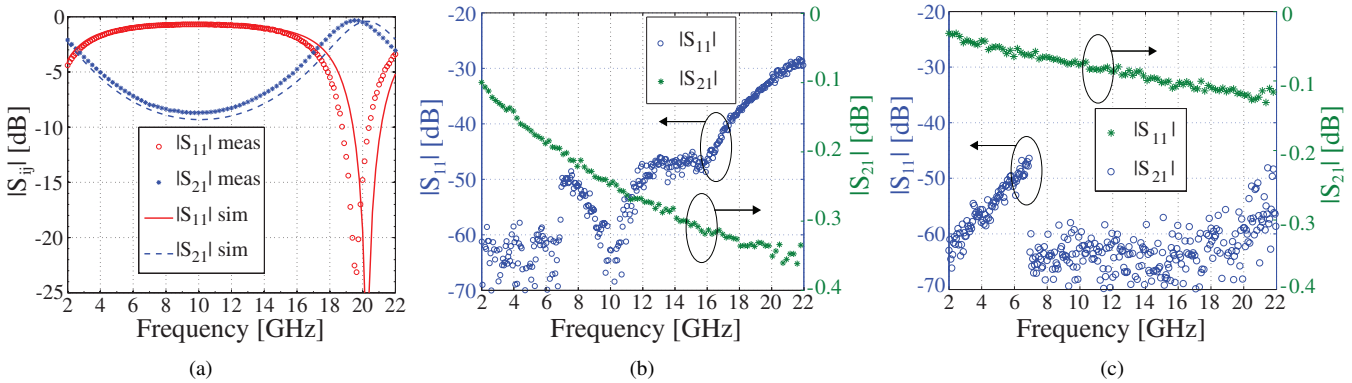


Fig. 4. (a) Simulation versus measurement results of an 8 Ω line with 50 Ω input and output ports. (b) Measured validation of the low-frequency TRL standard. The design frequency of this standard is 2 GHz–7 GHz. (c) Measured validation of the high-frequency TRL standard. The design frequency of this standard is 7 GHz–22 GHz.

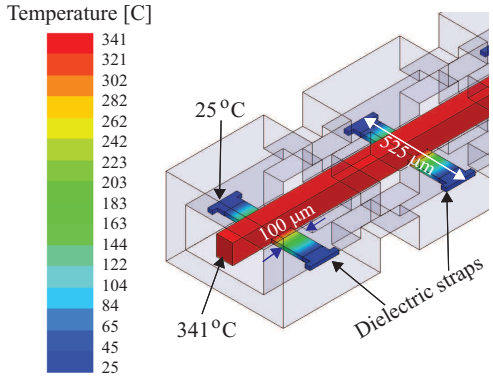


Fig. 5. This figure shows the static thermal simulation result of the five-layer low-frequency TRL line standard. The simulation is performed with Ansoft ePhysics™ for input power of 20 W. The temperature of the inner conductor increases to 341 °C, while the outer conductor temperature is kept at 25 °C.

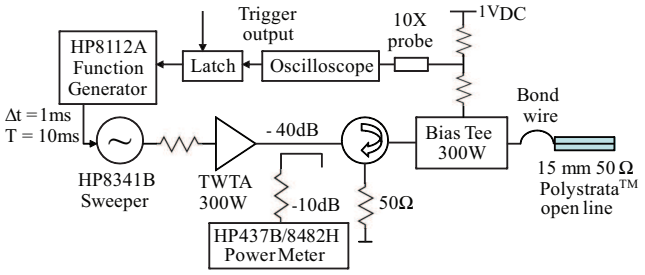


Fig. 6. Measurement setup for rf field breakdown testing performed with an open-ended 50 Ω line with up to 300 W of input power at 10 % duty cycle (1 ms duration pulses). Ionization provides a dc path through the bias tee. The detection of arcing automatically turns off the rf source, protecting the micro-coaxial line and allowing multiple tests.

Electric field breakdown was estimated based on HFSS™ simulations of the electric field distribution, which show that the transverse field distribution in the case of the 8 Ω line is the strongest in the narrow air gaps, while for the 50 Ω line the field is the strongest at the inner conductor corners. Table II gives the calculated maximum electric field magnitudes for 1 W of input power from a matched generator, indicating that the low-impedance lines and smaller lines are more sensitive to breakdown. For higher power levels, $|E_{\max}|$ can be obtained by multiplying the results in the table by $(P_{\text{in}}/1\,\text{W})^{1/2}$.

Power handling at 2 GHz was tested on a 15 mm long 50 Ω five-layer open-ended line, connected with a bond wire to a 0.085" (2.16 mm) diameter semi-rigid coaxial cable. Up to 12.6 W of CW power, resulting in 78 V estimated at the open end was input to the line for 45 min with no observed degradation.

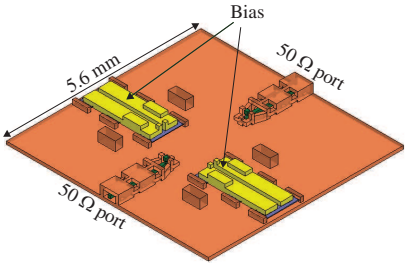
Up to 300 W of 10 % duty cycle 10 ms period pulsed power was input into a 15 mm line using the test setup shown in Fig. 6. These measurements reduce thermal stress on the open-ended micro-coaxial line, while enabling rf field breakdown testing up to 18 GHz. When voltage breakdown occurs, ionization creates a path for dc current to flow through the bias tee choke, creating a voltage drop measured by the oscilloscope with trigger set on a falling edge. When the oscilloscope triggers, the latch output resets, turning off the pulse generator. When the modulation is not present, the sweeper turns off, thus detecting breakdown and protecting the micro-coaxial line from damage. No arcing was detected at the test frequency of 2.5 GHz for power levels below 53 W, the level when a single arc occurred. Multiple arcs were observed at 120 W and 150 W, and arcing at 300 W resulted in catastrophic failure. Based on simulations and previous work by Woo [10], breakdown will likely not occur for an ideal micro-coaxial line until 120 W. The lower power level at which breakdown occurred is presumably due to an imperfect conductor surface.

TABLE II
CALCULATED MAXIMUM ELECTRIC FIELD, $P_{\text{IN}} = 1$ W

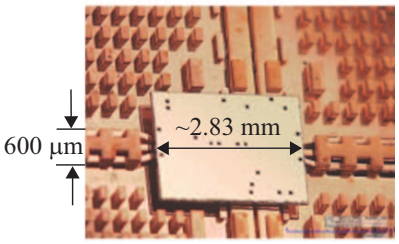
Line	5 layer 8 Ω	5 layer 50 Ω	11 layer 8 Ω	11 layer 50 Ω
$\lvert E_{\max}\rvert$ [V/m]	$1.13 \cdot 10^5$	$2.94 \cdot 10^5$	$0.99 \cdot 10^5$	$0.82 \cdot 10^5$

IV. Active Device Integration

The PolyStrata™ process allows integration with active devices. Depending on the type of integration, e.g., flip-chip or wire-bond, different "active sockets" need to be designed in order to compensate for parasitics. For the five-layer process, Ansoft HFSS™ was utilized to design a socket for flip-chip assembly of a distributed amplifier gain block comprised of a 600 µm gate periphery GaN HEMT MMIC on SiC. The design shown in Fig. 7 (a) includes a pair of two-wire bias lines for the gate and drain biases, and 50 Ω input and output ports. This socket is designed to match the 1–10 GHz operation range of the MMIC. Fig. 7 (b) shows the fabricated socket assembled with the active device. The solid and dashed lines in Fig. 8 show the simulated insertion and return loss of the socket with a flip-chipped 50 Ω microstrip line designed on a 100 µm thick SiC substrate. The value of $|S_{21}|$ is 0.05 dB at 10 GHz. Comparison of the measured small-signal performance of both the chip on wafer and in PolyStrata™ (Fig. 8) confirms that there is no degradation in active device performance when it is hybridly integrated in the monolithic micro-coaxial environment.



(a)



(b)

Fig. 7. (a) HFSS model of the socket, including 50 Ω input and output ports and two bias lines for gate and drain bias. (b) photograph of the active device flip-chipped to the socket. Conductive epoxy is used for electrical and mechanical connections.

In summary, this paper demonstrates properties of the TEM micro-coaxial lines, including wide impedance range, dc current handling, CW and pulsed rf power handling, and high-performance integration with MMICs. These results open the possibility for PolyStrata™ integration with high power active devices for broadband hybrid-monolithic ultra-compact solid-state power amplifiers.

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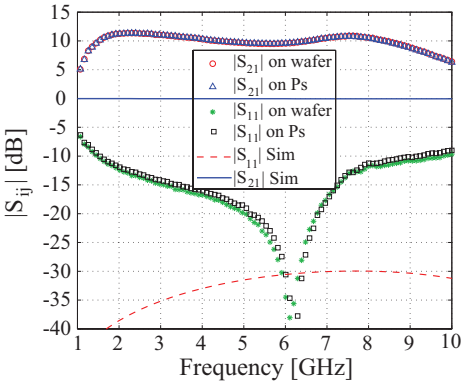

Fig. 8. Measured small-signal performance of the GaN on SiC MMIC with standard on-wafer probes compared to the performance of the same MMIC in the PolyStrata™ micro-coaxial environment. Simulation results of the socket with a 50 Ω microstrip line on a 100 µm thick SiC substrate are shown in solid and dashed lines.

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