Custom IC for Ultra-low Power RF Energy Harvesting

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Abstract—This paper presents a custom IC that provides an efficient interface between an ultra-low power RF rectifying antenna (rectenna) source and a microbattery, with the goal of maximum power harvesting. The energy harvester IC uses current-starved circuitry, a non-overlapping gate-drive, and a sub-threshold current source to achieve a nominal supply current in the 200 nA range for V_{DD} = 2.5 V. Experimental results are given with the IC harvesting energy from a 1.93 GHz patch rectenna to a battery with voltages ranging from 2.5 V to 4.15 V. Overall conversion efficiency including all control losses is demonstrated at over 35 % at an input power of just 1.5 µW and at over 70 % at input power levels over 30 µW. The IC is fabricated in a 5 V, 0.35 µm CMOS process. Although the IC was designed for RF energy harvesting, the low power boost converter can be applied to other power sources such as wind, vibrations, and temperature.

I. INTRODUCTION

As wireless sensor networks become more pervasive and sensor nodes operate at lower and lower average power levels, there is an increased need for low power energy harvesting techniques to provide power to the sensors. Previous work has shown sensors operating with a Texas Instruments MSP430 microcontroller in deep sleep mode with quiescent current consumption under 1.5 µA [1]. Controlling a power converter such that it presents a positive resistive load, also known as resistor emulation, has been shown to be a highly efficient method of harvesting maximum energy from a number of wireless power sources with a nearly constant output resistance ranging from RF to piezo-electric at very low power levels [2-6]. This method is advantageous at these very low power levels where traditional maximum peak-power tracking techniques cannot be used due to their higher power consumption or high input voltage requirement. Prior resistor emulation solutions have enabled wireless sensors to function indefinitely at input power levels as low as 100 µW [7]. However, systems built from commercially available discrete parts are limited by a minimum input power level before the converter control itself consumes more power than the wireless sensor. Another limitation is that the system cannot adapt to a new optimal load resistance over wider ranges of input power levels and varying sources. Thus, a custom integrated circuit (IC) is an improvement that further reduces power consumption and delivers useful energy to the wireless sensor at much lower input power levels. Some ultra-low power ICs have been able to harvest energy at very low input power levels [8], but they do not attempt to optimally load the input source for increased harvesting efficiency.

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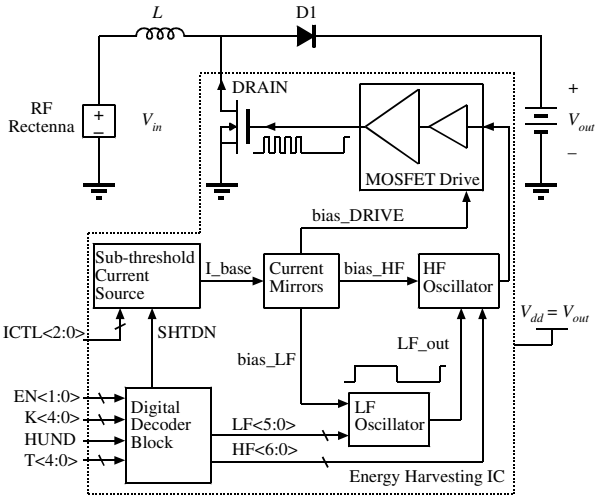


Figure 1: Block diagram showing the main components of the energy harvesting IC. Connections are shown between the on-chip power MOSFET and the remaining external components in a boost converter topology.

The energy harvesting IC presented in this paper is designed to emulate a wide range of programmable positive resistive loads to the input while transferring the energy with high efficiency to a wide range of battery voltages. The emulated resistance can be fixed or varied digitally depending on the attached wireless power source and input power level for optimal converter efficiency and maximum power delivered to the output. This paper first gives an overview of the energy harvesting IC in Section II, including design details on key circuit components. Experimental results of the IC in a boost-converter topology with an RF rectifying antenna (rectenna) as the wireless power source are provided in Section III demonstrating efficient energy harvesting with input power ranging from 265 µW down to less than 1 µW.

II. IC DESIGN OVERVIEW

A block diagram showing the general organization of the energy harvester IC is shown in Fig. 1. The on-chip power MOSFET can be the low-side switch in a boost or

non-inverting buck-boost converter depending on how the DRAIN pin is connected to the rest of the power stage. In Fig. 1, the IC is connected to a boost converter power stage. As is shown in [2-3], a boost converter operating in fixed-frequency pulsed discontinuous conduction mode (DCM), can emulate the positive resistance:

$$R_{em} = \frac{V_{in}^2}{P_{in}} = \frac{2 \cdot L}{D_1 \cdot t_1^2 \cdot k} \cdot \frac{M-1}{M} \text{ , where } M = \frac{V_{out}}{V_{in}}. \quad (1)$$

The control parameters are the converter filter inductance, L, the transistor on-time, t_1, the associated high-frequency duty cycle, D_1, and the low-frequency converter operation duty cycle, k. These parameters are derived from the filter inductor current waveform of a boost converter operating in pulsed DCM as shown in Fig. 2. The IC is designed for relatively low input voltages where the input voltage dependent term in (1), $(M-1)/M$, is essentially unity as $V_{in} << V_{out}$.

B. Sub-threshold Current Source

The sub-threshold current source provides an ultra-low base current (I_base) to the rest of the circuitry in the IC. This base current has a minimum value of 1.8 nA and is adjustable up to 10 nA via the digital control inputs ICTL<2:0>. The adjustable base current enables the IC to achieve a larger range of operating frequencies depending on the expected converter input power level.

A digital input of EN<1:0> = 00 disables the current source and thus brings the energy harvester IC into shutdown mode. A boot-strap circuit with an operating current of 100 pA restarts the current source in 7 ms when the IC is enabled.

C. Low-frequency Oscillator

The low-frequency (LF) oscillator block generates a low-frequency clock signal (LF_out) with an adjustable duty cycle, k, that pulses the high-frequency (HF) oscillator output on and off.

A simplified schematic of the LF oscillator is shown in Fig. 3. The oscillator uses a current control block to set the charge and discharge rate of a capacitor, C_{LF}, that increases and decreases the voltage on the capacitor respectively. The capacitor voltage varies within the hysterisis band of the a schmitt trigger.

All the circuitry is heavily current-starved in order to keep the power consumption of the energy harvester IC minimal. The current I_{LF} is scaled from the base current generated by the sub-threshold current source. The low-frequency duty cycle, k, is adjusted via digital inputs LF<5:0>. The digital bit LF<5> selects between a one current control block for high values of k and one for low values of k. This is done in order to allow for more precise control of the difference in capacitor charging and discharging current.

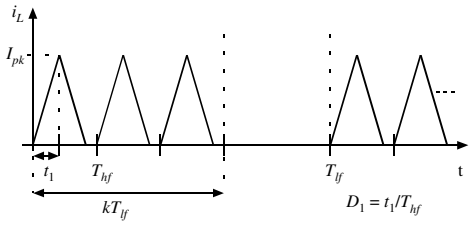


Figure 2: Current waveform of filter inductance, L, of a boost converter in pulse discontinuous conduction mode (DCM). The timing parameters t_1, D_1, and k, along with L define the converter emulated resistance, R_{em}.

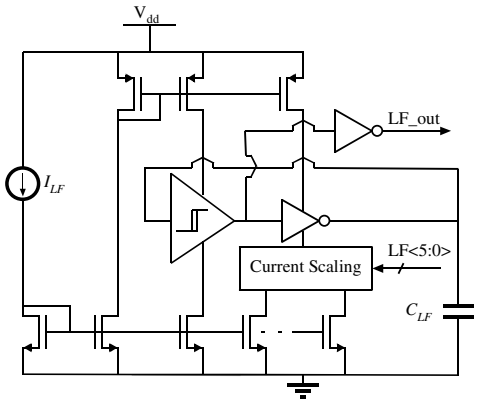


Figure 3: Simplified schematic of low-frequency oscillator circuitry. The current scaling block controls the current that discharges the timing capacitor, C_{LF}, and thus adjusts the k parameter.

In each of the two current control blocks, the capacitor charge current is set such that the HF oscillator is powered on long enough to output a sufficient number of switching periods for the converter to operate adequately. The remainder of the LF digital inputs, LF<4:0>, are used to change the amount of current that discharges C_{LF} and thus adjust the value of k. An additional digital input bit, HUND, is used to for $k = 1$. This bit disables the LF oscillator and provides the HF oscillator with a constant signal that keeps the HF oscillator output enabled and thus switching the on-chip power MOSFET at all times.

D. High-frequency Oscillator

The HF oscillator consists of three current-starved ring oscillators that generate a high-frequency signal (HF_out) with a fixed duty cycle of $D_1 = 50$ % and an on-time of t_1. This signal is then passed to the on-chip power MOSFET gate-drive circuitry. With the high frequency duty cycle fixed at 50 %, the equation for the emulated resistance (1) simplifies to

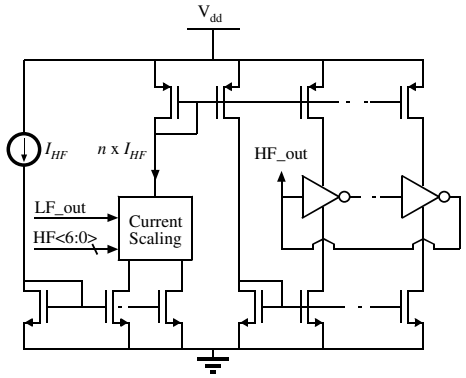


Figure 4: Simplified schematic of high-frequency oscillator circuitry. The current scaling block controls the current supplied into the elements of the current-starved ring oscillator and thus the t_1 parameter.

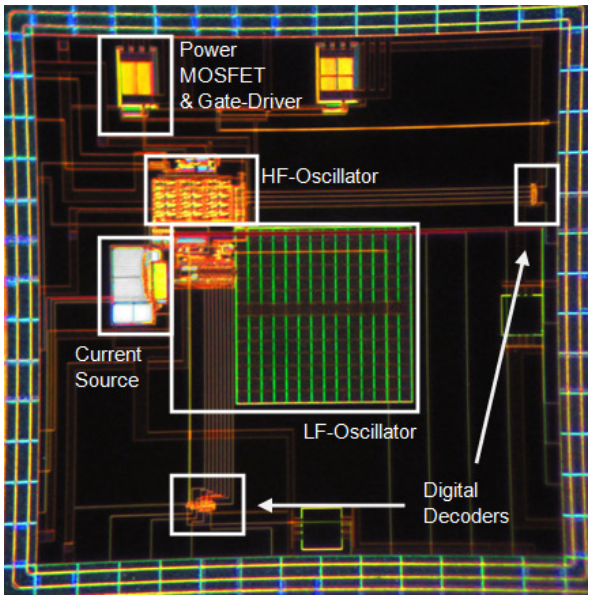


Figure 5: Microscope image of energy harvester IC fabricated in 5 V, 0.35 µm CMOS process. The various circuit components are labeled. The dimensions of the chip are: 2 mm x 2 mm.

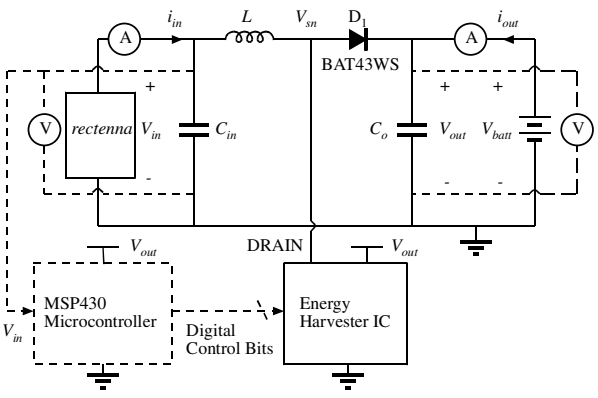


Figure 6: Schematic of experimental test setup for energy harvester IC used in a boost converter topology with an RF rectenna as the input power supply. The use of the IC along with an ultra-low power microcontroller is also investigated.

$$R_{em} = \frac{V_{in}^2}{P_{in}} = \frac{4 \cdot L}{t_1 \cdot k}, \text{ where } V_{in} << V_{out} \quad . \tag{2}$$

The three ring oscillators have different internal inverter sizes and thus have three different base values of t_1. The ring oscillator to be used is selected via EN<1:0>.

Fig. 4 shows a simplified schematic of one of these current-starved ring oscillators and a current scaling block. The digital inputs HF<6:0> set the scaling factor n of the HF oscillator base current I_{HF}. This adjusts the current fed into the ring oscillator and thus the frequency of its output.

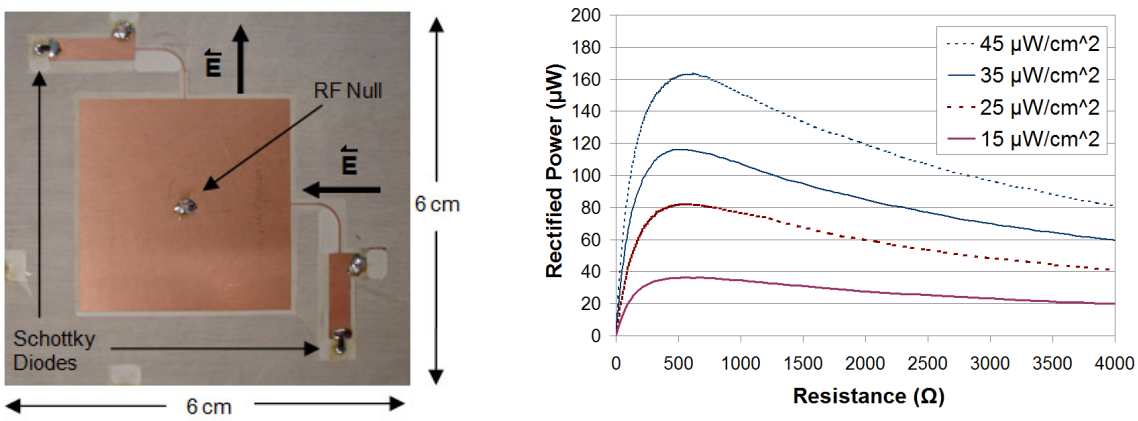
The output of the LF oscillator, LF_out, controls whether the ring oscillator is on or off. When LF_out is low, no current ($n = 0$) is supplied into the ring oscillator and the output, HF_out is pulled low.

E. Additional Circuit Components

The additional features in the energy harvester IC include a non-overlapping MOSFET gate-drive chain that eliminates IC power consumption from shoot-through currents. The on-chip power MOSFET sizing and gate-drive chain tapering is designed for optimal efficiency of a converter operating at sub-100 µW input power levels. The optimization is done with a modified process similar to that shown in [9]. The on-chip power MOSFET has an on resistance of $R_{ds\_on} = 2.1$ and an estimated gate capacitance of $C_{gs} = 1.19$ pF. The energy harvester IC was fabricated in a 5 V, 0.35 µm CMOS process. Fig. 5 shows a microscope image of the IC die and the various circuit components are labled. A 5 V process is used so that the IC can operate at most common battery voltages, including thin film lithium battries that have a nominal voltage of $V_{batt} = 4.15$ V [10].

III. EXPERIMENTAL RESULTS

The fabricated energy harvester IC is tested in a boost converter topology using the experimental setup shown in Fig. 6. The IC is powered directly from the converter output, V_{out}. The input and output capacitors, C_{in} and C_{out}, are 60 µF and 20 µF respectively. The total output current, i_{out}, to a voltage source simulating a battery, V_{batt}, is measured using a calibrated Agilent 34411A multi-meter. This output current includes the current consumption of the energy harvester IC along with the converter output current. The measured current consumption of the IC over the full range of timing control settings is given in Sect. III.B. below. Section III.C presents experimental results of the IC used to harvest energy from an RF rectenna power source. Use of the energy harvester IC together with a low power Texas Instruments MSP430 microcontroller for auto-tuning and configuration is discussed and experimental results are presented in Sect. III.D.



(a) (b)

Figure 7: a) Image of a 6 cm x 6 cm 1.93 GHz dual-polarized patch rectenna. b) Power curves for the patch rectenna over a family of incident power densities (W/cm^2). The power curves indicate an optimal load of R_{em} = 500 . The incident wave is linearly polarized along one of the polarizations. Similar power curves are measured for the other orthogonal polarization.

A. *RF Rectifying Antenna*

The RF energy harvesting component consists of an antenna integrated with a rectifier, and is referred to as a "rectenna". One or more incident waves are received by the patch antenna shown in Fig. 7a. This antenna receives independently, power contained in two orthogonal linear wave polarizations in order to maximize the average received power in a multipath fading propagation channel. The antenna is designed to operate in the 1.93 GHz band. Since the wavelength in free space is 15.5 cm, in order to reduce the size of the antenna, a high dielectric constant substrate was used, resulting in a 6 cm x 6 cm total area, including the ground plane. Two Skyworks SMS7630 GaAs Schottky diodes are connected at the high-impedance radiating edges of the antenna and rectify the power received in the two polarizations indicated in the figure. The diodes were characterized using a Focus Microwave load-pull setup and were determined to operate well with high-impedance RF loads at low incident power levels. The center of the patch antenna is an RF voltage null, and therefore the DC output can be taken from this point through a via to the back side, with good RF-DC isolation. Several such rectenna elements can be combined in an array for larger area power collection.

Fig. 7b shows a family of measured power curves for the rectenna at 1.93 GHz, where the rectified DC power is plotted as a function of DC load resistance for various power densities at normal incidence and in one polarization. The power density is calibrated with a known-gain antenna placed in the far field of the patch and fed by a RF source and amplifier. To estimate the RF-to-DC efficiency, the incident power density is multiplied by the total antenna geometric area. For 45 μW/cm^2 power density, a total of 1620 μW is incident on the antenna geometric area, resulting in 10 % RF conversion efficiency. Note that this is a conservative estimate, since the effective area of an antenna is always smaller than its geometric area. For low incident power densities, the efficiency decreases since the diodes are operated outside of the non-linear part of the IV curve, and since the diodes have a finite turn-on voltage.

B. *Energy Harvester IC Experimental Timing*

The energy harvester IC is tested alone to measure the quiescent control current consumption for each timing parameter. The digital inputs to the IC are swept to find the achievable timing parameters and associated current consumption at three sample battery voltages (2.5 V, 3.3 V, and 4.15 V).

The k parameters that the IC is able to generate are plotted in Fig. 8 over three supply voltages and with t_1 = 25 μs. These parameters range from k = 0.03 to k = 1. As can be seen in the plot, there are two distinct curves at each voltage level. The two curves correspond to the two different current control blocks in the LF oscillator design: low k and high k. Each curve is linear as the HF oscillator timing is fixed and increasing k is essentially increasing the percentage of time over a low-frequency period that the HF oscillator is enabled and consuming power. There is a higher resolution between k selections in the low k curve by design, as the energy harvester IC is designed for relatively low input power levels where a low k parameter is required for achieving good boost converter efficiency. For k = 1, the low frequency oscillator is disabled and the HF oscillator is on constantly.

Varying the supply voltage while keeping LF<4:0> fixed does not affect the k control parameter significantly as the current ratios in the LF oscillator remain the same. The low-frequency period will change with V_{batt} as the hysteretic band of the current-starved Schmitt trigger will vary with the supply voltage.

In Fig. 9, a sample of the achievable t_1 control parameters is presented for three supply voltages. The full range of transistor on times is 0.5 μs < t_1 < 80 μs for V_{batt} = 4.15 V. The associated current measurement is given with k = 1.

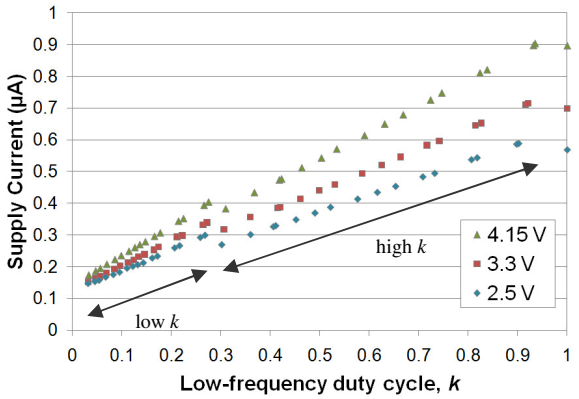


Figure 8: Achievable low-frequency duty cycle parameter, k, and the associated energy harvester IC supply current for three different supply voltages. The supply current includes the power consumption of the HF oscillator operating at $t_1 = 25$ µs.

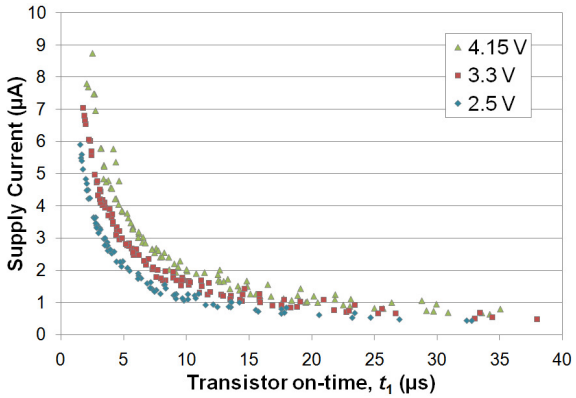


Figure 9: Sample of transistor on-times, t_1, that the HF oscillator can output and the associated supply current for three different supply voltages while $k = 1$. The full range of transistor on-times is 0.5 µs < t_1 < 80 µs.

For fixed digital inputs EN<1:0>, ICTL<2:0>, and HF<6:0>, t_1 will vary with V_{batt} due to the change in absolute currents and the propagation delay of an individual current-starved inverter in the ring-oscillator chain.

For an example filter inductance, $L = 330$ µH, and $D_1 = 0.5$, the range of k and t_1 available results in a large range of achievable emulated resistances based on (1), ranging from 16.5 < R_{em} < 88 k .

C. *Fixed Emulated Resistance Timing*

Next the energy harvester IC is tested in a boost converter power stage with the DRAIN pin connected to the converter switch-node, V_{sn}, of Fig. 6. The secondary switch is a Schottky diode (BAT43WS) with a nominal forward voltage drop of $V_D \approx 0.35$ V. The input power source is the RF rectenna described in Sect. III.A. To select the value of the external filter inductance, L, and the timing parameters, k and t_1, the design procedure in [2] is modified for losses specifically associated with the energy harvester IC.

Total power losses of the boost converter and the IC are still defined as the sum total of conduction, switching, and control losses:

$$P_{loss} = P_{cond} + P_{sw} + P_{ctrl}, \text{ where}$$

$$P_{ctrl} = P_{fix}\left(k, f_{lf}\right) + P_{pwm}\left(f_{hf}\right) \cdot \; k + \frac{t_{settle}}{T_{lf}} \qquad (3)$$

The value of P_{fix} for the energy harvester IC is determined from the results in Fig. 8. At a given supply voltage, the current consumption of just the LF oscillator, current source, and current mirrors is the y-axis intercept of a linear trend line created from the series of k parameters and corresponding supply current. For $V_{batt} = 2.5$ V, the current consumption using the low k current control block is 110 nA and for the high k current control block, it is 115 nA. Therefore, $P_{fix} = 275$ nW and 287 nW for low and high k parameters respectively at $V_{batt} = 2.5$ V. The current consumption of the LF oscillator, current source, and current mirrors do not change significantly with V_{batt}.

For a given supply voltage, a piecewise linear equation is used to trace the curve formed by the corresponding t_1 and supply current combinations. It is then used in efficiency optimization simulations as $P_{pwm}(t_1)$. Note that the HF oscillator in the IC has a settling time of approximately 40 µs, which is considered small enough to ignore ($t_{settle} << T_{lf}$).

In addition to editing P_{fix} and P_{pwm} in converter efficiency optimization simulations, switching power losses associated with the on-chip power MOSFET gate capacitance, C_{gs}, are removed from P_{sw} as these are now included in P_{pwm}.

With the modified boost converter power loss equations in place, efficiency optimization calculations for $R_{em} = 500$ result in the selection of $L = 330$ µH as the discrete filter inductor in the boost converter power stage. This value provides the best maximum possible converter efficiency (variable t_1 and k) for a range of low input power levels (1 µW ≤ P_{in} ≤ 150 µW). Next, the timing parameters are selected to optimize efficiency for a specific input power level.

First, the minimum input power level, P_{in}, at which efficient energy harvesting is possible is investigated. To optimize efficiency and for $R_{em} = 500$ at $P_{in} = 1$ µW, the timing parameters $t_1 = 32$ µs and $k = 0.083$ are selected and a supply voltage of $V_{batt} = 2.5$ V is used. With these fixed R_{em} and timing parameters, the incident power to the RF rectenna input source is swept and the resulting input powers, input voltages, emulated resistances, output powers, and converter efficiencies are found and plotted in Fig. 10. The resulting efficiency plot versus input power shows converter efficiencies above 10 % at $P_{in} < 1$ µW. However, although the converter can harvest energy efficiently at ultra-low P_{in}, the maximum converter efficiency at higher input power levels is just above 60 %. Therefore, to demonstrate higher converter efficiencies at other P_{in}, the input power sweep is repeated for three other timing parameter combinations:

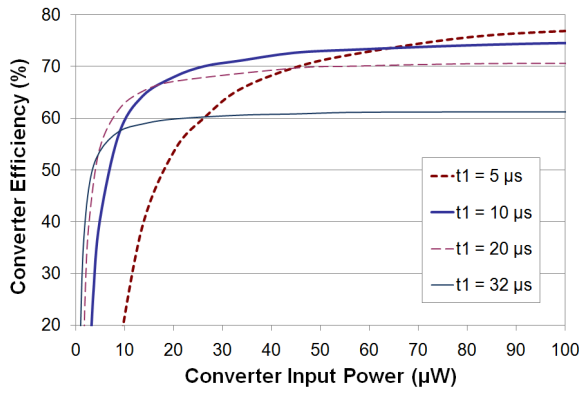


Figure 10: Efficiency curves of the energy harvester IC in a boost converter topology at four different control timing parameter combinations (t_1, k). Each combination optimizes converter efficiency for four different input power levels and for R_{em} = 500 .

(t_1 = 20 µs, k = 0.13), (t_1 = 10 µs, k = 0.26), and (t_1 = 5 µs, k = 0.50), for P_{in} = 5 µW, 30 µW, and 80 µW respectively. The resulting plots in Fig. 9 show improved converter efficiency at the desired P_{in} for the selected timing parameter combination in comparison to the other three.

In Fig. 11, the maximum possible converter efficiency, with manual optimization of timing parameters, is plotted. That data is also presented in Table I. The same experiment is repeated at V_{batt} = 4.15 V with L = 330 µH and the desired emulated resistance remaining, R_{em} = 500 . The resulting data can be found in Table II.

Note that in both experiments, the experimental R_{em} remains within 10 % of the desired value. The converter efficiency at the higher V_{batt} is worse at low P_{in} as expected due to the increase in energy harvester IC power consumption. However, at higher input power levels, the converter efficiencies are comparable due to the reduced significance of control power losses.

These results show that with the energy harvester IC presented in this paper, the minimum P_{in} at which energy can be harvested from a wireless power source is over a decade lower than systems using discrete hardware [2-3].

D. Microcontroller Controlled Emulated Resistance Timing

In order for the energy harvester IC to adjust the boost converter control timing parameters, t_1 and k, to optimize converter efficiency over multiple magnitudes of input power level, it is used in conjunction with an ultra-low power Texas Instruments MSP430 microcontroller.

The microcontroller provides the digital control bits to the energy harvester IC and operates in sleep mode for the majority of the time with the on-board very low power VLO oscillator (12 kHz) enabled. The oscillator feeds a timer that counts up to a user-defined value that determines how often the microcontroller ADC (10-bit SAR) wakes up and samples the converter input voltage. Once the conversion is complete, the ADC powers down automatically. The converted input

TABLE I
EXPERIMENTAL RESULTS WITH
MANUAL ADJUSTMENT OF R_{EM} (V_{DD} = 2.5 V)

$P_{incident}$ (µW/cm^2)	P_{in} (µW)	V_{in} (mV)	R_{em} ( )	P_{out} (µW)	$_{boost}$ (%)
1.29	0.89	20.90	489	0.16	18.05
1.74	1.48	26.85	489	0.52	35.13
2.51	2.73	36.45	488	1.29	47.36
3.55	4.80	48.40	487	2.57	53.58
6.92	13.51	81.60	493	8.81	65.16
12.9	33.54	132.4	523	23.86	71.14
24.6	80.13	202.7	513	60.66	75.70
30.3	104.7	231.8	513	80.77	77.13
41.6	156.3	283.9	516	123.6	79.06
63.9	265.0	376.0	534	211.5	79.80

TABLE II
EXPERIMENTAL RESULTS WITH
MANUAL ADJUSTMENT OF R_{EM} (V_{DD} = 4.15 V)

$P_{incident}$ (µW/cm^2)	P_{in} (µW)	V_{in} (mV)	R_{em} ( )	P_{out} (µW)	$_{boost}$ (%)
2.07	1.96	31.70	513	0.25	12.73
2.51	2.72	37.30	512	0.77	28.43
3.55	4.79	49.45	511	2.18	45.52
5.2	8.66	66.50	511	4.73	54.64
6.92	13.30	82.60	513	7.96	59.82
9.01	20.33	103.8	530	13.34	65.61
12.9	31.18	128.7	531	21.61	69.3
24.6	78.71	194.2	479	57.59	73.16
58.4	237.5	332.0	464	181.8	76.55
73.5	306.8	376.0	460	241.5	78.72

TABLE III
EXPERIMENTAL RESULTS WITH
MICROCONTROLLER ADJUSTMENT OF R_{EM} (V_{DD} = 2.5 V)

$P_{incident}$ (µW/cm^2)	P_{in} (µW)	V_{in} (mV)	R_{em} ( )	P_{out} (µW)	$_{boost}$ (%)
2.51	2.80	37.21	494	0.13	4.47
3.55	4.06	44.60	490	0.88	21.56
4.23	5.25	51.20	500	1.49	28.34
5.20	8.89	66.21	493	4.30	48.42
9.01	19.89	102.4	527	12.50	62.86
10.9	26.13	116.1	516	17.23	65.91
12.9	38.61	138.9	500	26.80	69.40
24.6	81.07	205.2	520	37.23	72.19
30.3	102.3	227.6	506	76.95	75.22
63.9	273.4	372.5	507	216.3	79.09

voltage value is used in a look-up table to adjust the digital control bits sent to the energy harvester IC and the converter timing changes accordingly. Note that this tracking scheme requires prior knowledge of the input rectenna source characteristics and also requires the energy harvester IC to be accurately emulating a known resistance.

The desired frequency at which the microcontroller samples the converter input voltage depends on the environment that the energy harvesting IC is operating in. There is a trade-off between the microcontroller tracking speed of the input power level that is required for areas with quickly varying RF fields, and the acceptable increase in control power loss. P_{fix}, that has to be minimized in areas with very low incident RF power.

For the experimental results presented in Fig. 11 and Table III, the microcontroller sampling period is set at 1 s to

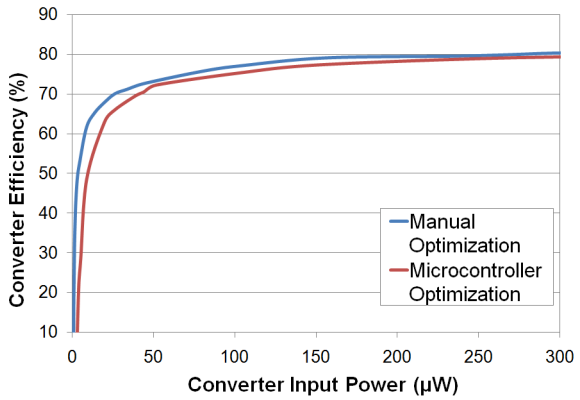


Figure 11: Efficiency curves of the energy harvester IC in a boost converter topology with manual and microcontroller optimization of control timing parameters, t_1 and k.

minimize the increase in control power consumption. At a tracking frequency of 1 Hz, the microcontroller has a supply current of 375 nA. The new values of P_{fix} with the energy harvester IC and microcontroller combined for high and low k is 1225 nW and 1212.5 nW respectively (V_{batt} = 2.5 V).

The increase in P_{fix} is evident in the efficiency plot of the energy harvester IC with microcontroller optimization shown in Fig. 11. At very low converter input power levels, the converter efficiency is greatly reduced. However, as P_{in} increases, the control power loss becomes a much smaller percentage of total power loss, and thus the increase in P_{fix} from the addition of the microcontroller has a negligible impact on converter efficiency.

IV. CONCLUSION

An energy harvester IC that uses resistor emulation to optimally load an RF rectenna wireless power source has been shown to deliver usable power at input power levels as low as 1.5 W at converter efficiencies, $_{boost}$, over 35 %. The IC uses simple, current-starved analog circuitry to be able to control a boost or buck-boost converter in fixed-frequency DCM operation and thus achieve a desired emulated resistance within the range: 16.5 $\leq R_{em} \leq$ 88 k . Experimental results demonstrate the energy harvester IC in a boost converter topology maintaining an emulated resistance within 10 % of a designed value with fixed converter control timing parameters, t_1 and k, over a decade of input power levels, P_{in}. To maximize energy harvesting over a wider range of P_{in}, the converter control timing parameters are tuned using a Texas Instruments MSP430 microcontroller together with the energy harvester IC.

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