Harmonic Load Pull of High-Power Microwave Devices using Load Pull Tuners

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Abstract—This paper presents a high-power high-efficiency PA design method using gradient tuning at fundamental-frequency load pull tuners. Harmonic impedance control at the virtual drain is accomplished through the use of tunable pre-matching circuits and full-wave EM modeling of package parasitics. A GaN transistor from Cree is characterized using the method and load-pull contours presented to illustrate the dramatic impact of varying 2nd and harmonic termination. A 3rd harmonic termination is added to satisfy conflicting class-F and F^{-1} load pull results in maximum efficiency improvement over the best-case 2nd harmonic termination. The method is verified by designing and measuring a 36-W class-F^{-1} PA prototype at 2.1 GHz with 81% drain efficiency and 14.5 dB gain (71% PAE) in pulsed operation.

Index Terms — harmonic load pull, class-F, inverse class-F

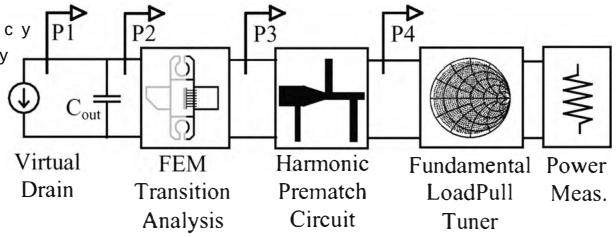


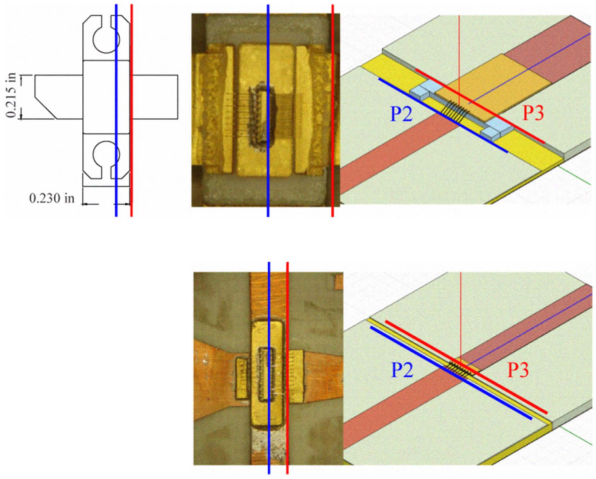
Fig. 1. Block diagram of the output portion of a load-pull system for characterization of a transistor's virtual drain (P1) impedance at the device reference plane. Harmonic impedance control (P3) is accomplished through the use of tunable pre-matching circuits and full-wave EM modeling of package parasitics (P2). Fundamental load pull (P4) is used to characterize the transistor's virtual drain impedance.

I. Introduction

High-efficiency microwave power amplification is achieved by shaping transistor voltage and current waveforms across the active device [1]. For example, odd-harmonic open circuit and even-harmonic short circuit terminations result in squaring of the drain voltage waveform and peaking of the drain current waveform [2]. Class-F (voltage squaring) operation has been used to achieve more than 80% PAE at 2 GHz with 16.5 W output power [3] by controlling impedance at the 2nd, 3rd, and 4th harmonic. [4] suggests that Class-F^{-1} (current squaring) operation provides benefits including higher fundamental load impedance and reduced sensitivity to transistor on-resistance. Class-F^{-1} also benefits from strong 3rd harmonic drain current components generated when the drain voltage descends below the knee voltage [5].

Most non-linear transistor models fail to accurately reproduce transistor behavior at harmonic frequencies and under heavy gain compression. In other cases nonlinear models are not available. Therefore, load pull [6] is commonly used in conjunction with analytical methods in the design of high-power PAs. Traditional load pull makes use of mechanical tuners to vary drain and gate impedance. Transistor performance is measured over a constellation of fundamental frequency impedances while harmonic impedances are allowed to vary arbitrarily. Elaborate active and passive harmonic load pull techniques [7] are available but are less common and significantly more expensive.

In this paper we describe a simple, low cost method for control and systematic variation of harmonic impedances based on the block diagram of Fig. 1. By convention, fundamental frequency output impedance is referenced to plane P3 and harmonic frequency impedances are referenced to plane P1. This reference plane is intrinsic to the device at the output of the transconductance, and is referred to as the virtual drain. Harmonic terminations must be referenced to this plane to achieve the high-efficiency modes described in the literature. Fig. 2 shows the position of reference planes P2 and P3 from Fig. 1 for two packaging configurations. Full-wave electromagnetic analysis of these configurations, presented in Section 2, is used to calculate the impedance at the



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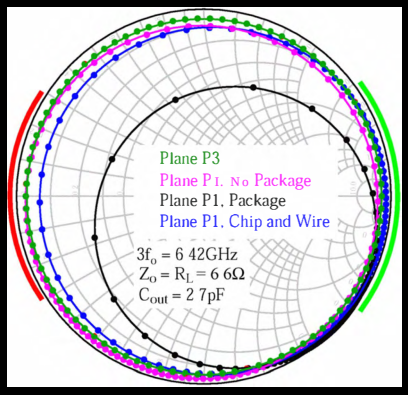
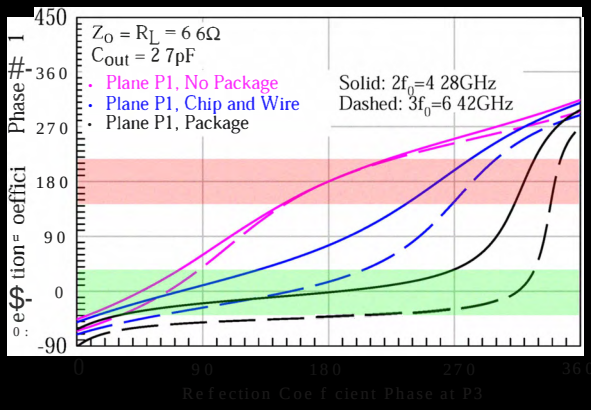
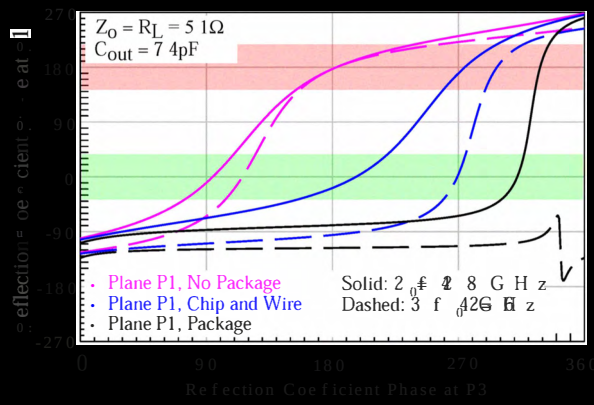

Plane P3
Plane P1, No Package
Plane P1, Package
Plane P1, Chip and Wire
3f0 = 6.42GHz
ZO = RL = 6.6Ω
Cout = 2.7pF


ZO = RL = 6.6Ω
Cout = 2.7pF
Plane P1, No Package
Plane P1, Chip and Wire
Plane P1, Package
Solid: 2f0=4.28GHz
Dashed: 3f0=6.42GHz
Phase #-
450
360
270
180
90
0
-90
0
90
180
270
360
Reflection Coefficient Phase at P3


ZO = RL = 5.1Ω
Cout = 7.4pF
Plane P1, No Package
Plane P1, Chip and Wire
Plane P1, Package
270
180
90
0
-90
-180
-270
0
90
180
270
360
Reflection Coefficient Phase at P3

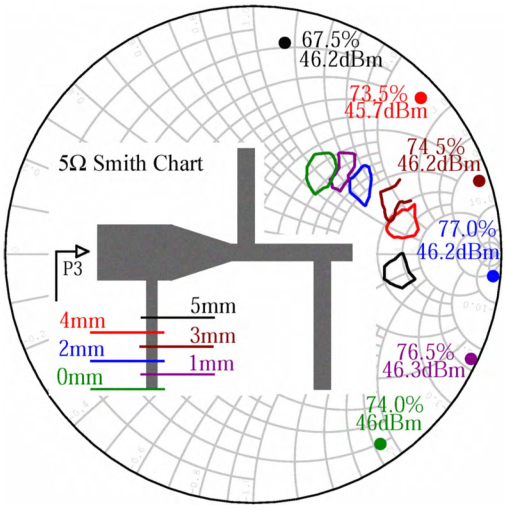


Fig. 6. Fundamental frequency load contours and efficiency contours (referenced to P3) showing color shift corresponding to 2nd harmonic termination, with peak efficiency and maximum power for each contour indicated next to corresponding marker.

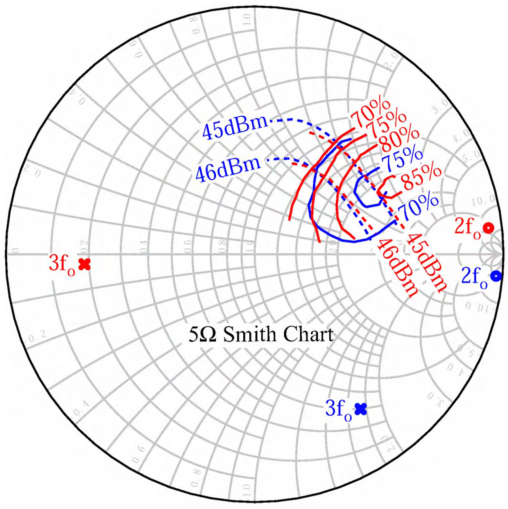


Fig. 7. Power (red) and drain efficiency (blue) vs. load impedance at the current generator plane for two different harmonic terminations, corresponding to the 2nd harmonic open and short circuit terminations, respectively. Both sets of 2nd (o) and 3rd (x) harmonic impedance terminations are referenced to the package reference plane.

to achieve each harmonic termination. The highest efficiency region (77 %) is achieved with 2nd harmonic nearest an open circuit (blue). In this case the 3rd harmonic was not explicitly controlled, but was fixed at a capacitive impedance.

Next we investigate the impact of 3rd harmonic control. Another output prematch circuit was designed to terminate 2nd and 3rd harmonics in an open and short at P1, respectively (the class-F^{-1} condition). Fig.7 compares results from this measurement to the 2nd-harmonic-only measurement of Fig. 6. Intentional termination of the 3rd harmonic increases transistor drain efficiency by 8 % without reducing output power.

A prototype PA was designed using results of the measurements in Fig. 7, shown in shown in Fig. 8. A fundamental load impedance of $10.+2j6.2\Omega$ was presented at plane P3

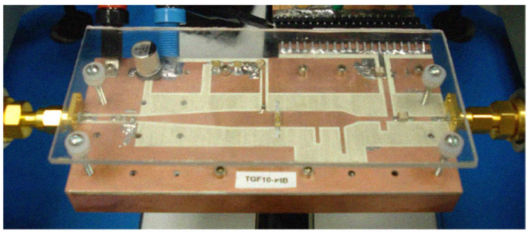


Fig. 8. Photograph of fabricated 36-W dual-stage PA prototype with 81% drain efficiency and 14 GHz.

with 0.27 dB insertion loss in the output matching circuit. 2nd and 3rd harmonic impedances approximate an open and short at plane P1 similar to those shown Fig. 7. Output power of 36 W was measured with 14.5 dB gain and 81 % drain efficiency, or 78 % PAE at 2.14 GHz, consistent with load pull characterization results.

V. Conclusion

The analysis in Section 2 shows that harmonic terminations of high-performance devices can be impacted by output matching. In such cases the results of Section 4 indicate that transistor performance will change significantly based on the harmonic environment. A method has been presented to systematically sweep harmonic termination, resulting in a very high-efficiency class-F^{-1} PA prototype.

VI. Acknowledgements

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