System Considerations for Efficient and Linear Supply Modulated RF Transmitters

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***Abstract*—This paper presents an overview of the envelope tracking RF transmitters which require a dynamic power supply implemented as an envelope modulator. Optimal design of this component requires an understanding of the system and power amplifier (PA) behavior. Here, we specifically address design of transmitters for wireless communications at the base station in the 2.14 GHz band with W-CDMA modulation. PA characterization and a new system modeling method are developed to determine envelope modulator requirements for a given signal type. System measurements of a proof-of-concept ET system dissipates 61 % less power than the traditional drive-modulated transmitter.**

I. Introduction

Final stage power amplifier (PA) efficiency and linearity dominate performance of a typical RF transmitter. Linearity is required by FCC regulations and to maintain link performance, and high efficiency is important to extend battery life, decrease energy costs, and simplify thermal management. PAs achieve increased efficiency near maximum output power when operating in gain compression, but efficiency drops quickly with reduced output power. Typical behavior for a high-efficiency PA (described in [1]) is shown by the solid line in Fig. 1. High-efficiency design techniques achieve dramatic efficiency enhancement, but only near peak output power.

Communication systems require variation of average output power to maintain link quality and reduce energy consumption. Furthermore, modulation schemes targeting spectral efficiency use output power variation to transmit information [2]. For example, GSM cellular networks use Gaussian minimum shift keying (GMSK) modulation which has no power variation, but output power is varied widely with each 577 μsec timeslot to accommodate the needs of different users. By contrast, signals used by the wideband code division multiple access (W-CDMA) for downlink (base-station to mobile) transmission in many 3G cellular networks have peak to average power ratio (PAR) of 6 dB to 10 dB. Average power of W-CDMA signals also varies with network traffic [3]. The probability distribution for a 7 dB PAR W-CDMA downlink signal with 39 dBm average power is shown in the histogram of Fig. 1.

Operated at V_{dd}=32V, the high-efficiency PA produces peak output power (46 dBm) with 76 % efficiency, but the average output power level (39 dBm) with only 32 % efficiency. If drain voltage were reduced to 16 V the average output power could

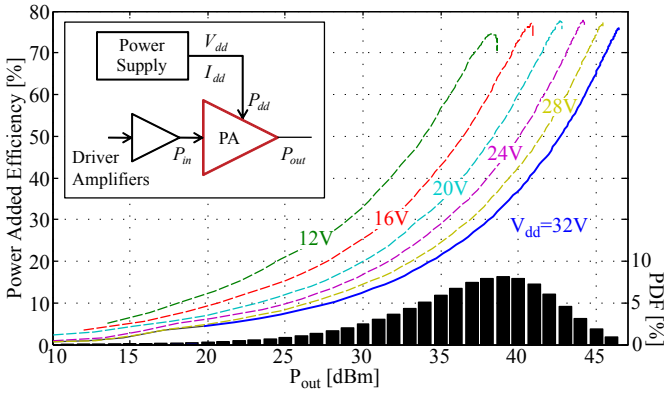

Fig. 1. Measured PAE vs. output power for a 2.14 GHz class-F^{-1} GaN HEMT PA for varying drain supply voltage (design of this PA is described in [1]). Probability density function of a 7 dB PAR W-CDMA downlink signal is shown in bars at the bottom.

be produced with nearly 70 % efficiency. Drain modulation systems use drain voltage to control output power, improving PA efficiency. The concept was originally introduced as Kahn Envelope Elimination and Restoration (EER) [4]. In the last decade several researchers (e.g. [5], [6]) have extended and refined the idea, making it suitable for use with high-PAR and high-bandwidth signals.

Referring to the block diagram of Fig. 1, an ET system requires a power supply which is dynamic - varying with output power. An additional component is required to perform drain voltage control in an ET transmitter. Here we refer to it as an envelope modulator (EM), which must meet several requirements:

- it must vary drain voltage with output power to make the PA efficient, this variation may be once every 577 μsec (GSM) or at many times the modulation bandwidth (W-CDMA);
- drive the PA drain resistance, which varies very quickly;
- control drain voltage precisely to maintain high transmitter linearity; and
- operate efficiently, because ET system efficiency includes both PA and EM efficiency ($\eta_{ET} = \eta_{PA} \times \eta_{EM}$).

The inter-related nature of the ET component requirements necessitate an understanding of PA behavior and a system-

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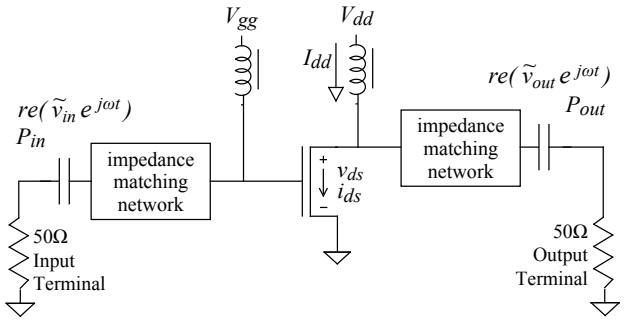


Fig. 2. Block diagram of a FET-based RF power amplifier. Matching networks are used to transform 50-Ω input and output terminal impedances to a specific complex RF impedance required to achieve the desired mode of operation. Bias networks, shown here as an inductance, isolates the RF transistor drain from the DC power supply at the RF frequency.

level approach to EM design.

In this paper we discuss system considerations for design of an ET system. Section 2 provides background on PA behavior and characterization of a simulated PA over a range of drain voltage and RF drive power. Section 3 describes the envelope tracking system design, and interaction between the EM and PA, and Section 4 discusses presents results of an integrated proof-of-concept envelope tracking system.

II. PA Behavior

The whole point of the ET system is enhancement of PA efficiency while meeting required linearity, so an understanding of system-level PA behavior is critical. ET transmitters bring together the fields of RF, analog and power electronics, and signal processing, so this section also serves to clarify important definitions.

The block diagram of a general PA based on a FET-type transistor is shown in Fig. 2. PA design considers device selection, fundamental and harmonic frequency gate and drain impedances, matching and bias circuit design, and bias conditions to achieve the desired gain, linearity, output power, and efficiency characteristics. Further detail on PA operation and design can be found in [7].

The basis for PA theory and operation is in analysis of drain-source voltage and current waveforms (v_{ds} and i_{ds}). The dominant source of inefficiency in traditional PA is transistor power dissipation, which occurs when drain-source voltage and current overlap in time. Therefore high-efficiency PA design is concerned with shaping these waveforms to avoid overlap while still maintaining a large fundamental frequency component. The output impedance matching network isolates the output terminal from the drain at harmonic frequencies, therefore only the fundamental-frequency energy appears at the output terminal.

At the system level, however, the PA can be viewed as a black box described by drain voltage, drain current, and the RF input and output, measured in a 50-Ω environment. The performance metrics presented in the next section provide a complete description of system-level PA behavior.

A. PA Performance Metrics

RF input and output power are defined as P_{in} and P_{out} at the 50Ω PA terminals. Amplitude and phase modulation of the carrier is described by complex baseband signals $\tilde{v}_{in}$ and $\tilde{v}_{out}$, where the tilde denotes complex baseband quantities. Power and baseband voltage magnitude are directly related by:

$$P_{in} = \frac{|\tilde{v}_{in}|^2}{100} \tag{1}$$

PA power gain is calculated as follows:

$$G = \frac{P_{out}}{P_{in}} \tag{2}$$

and is frequently expressed in decibels. PA envelope voltage gain is the relationship between input and output modulation. $\tilde{G}_v$ is complex, accounting for both gain and insertion phase:

$$\tilde{G}_v = \frac{\tilde{v}_{out}}{\tilde{v}_{in}} \tag{3}$$

The envelope voltage gain of an ideally linear PA is constant. The drain efficiency of a power amplifier is defined by the following:

$$\eta_d = \frac{P_{out}}{P_{dd}} = \frac{P_{out}}{V_{dd} \times I_{dd}} \tag{4}$$

High PA efficiency comes at the cost of reduced gain (or "gain compression"). PAE accounts for reduced gain (and the required increase of input power) and is therefore a more complete efficiency metric:

$$PAE = \frac{P_{out} - P_{in}}{P_{dd}} = \frac{P_{out}(1 - \frac{1}{G})}{P_{dd}} = \eta_d \left(1 - \frac{1}{G}\right) \tag{5}$$

Power supplied to the PA but not delivered to the output terminal is dissipated in the PA, matching networks, or bias networks as heat:

$$P_{diss} = P_{out} \left(1 - \frac{1}{G}\right) \left(\frac{1}{PAE} - 1\right) \tag{6}$$

B. Drain Bias Circuit

The bias network is designed to isolate the drain power supply from the RF circuit such that current I_{dd} and voltage V_{dd} in Fig. 2 have no RF component. Thus the PA can be viewed by the drain bias supply as a nonlinear resistance which varies with V_{dd} and $|\tilde{v}_{in}|$:

$$R_{dd} = \frac{V_{dd}}{I_{dd}} = \frac{V_{dd}^2 \eta_d}{P_{out}} = \frac{V_{dd}^2 PAE}{P_{out} - P_{in}} \tag{7}$$

Traditional and ET bias networks are shown in Fig. 3. The RF choke (RFC) is required to present very high impedance at the RF frequency to prevent the bias circuit from impacting RF performance. Additionally, the RFC must also present very low impedance at the modulation frequency so that I_{dd} can change quickly with output power variation. In a traditional (constant-V_{dd}) PA a bank of capacitors of various size and value typically follows the RFC, serving two purposes:

1) to present a low impedance to the PA at frequencies between the modulation and RF carrier frequencies, enhancing the stability of the RF transistor; and

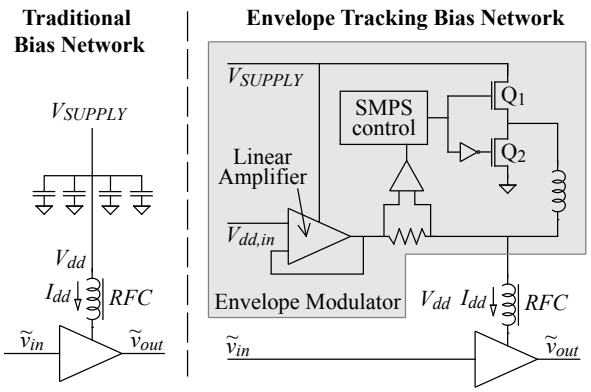


Fig. 3. PA drain bias circuit used for traditional (left) and ET (right) operation.

2) to present a low impedance to the PA at the modulation frequency, such that V_{dd} remains constant under fast changing I_{dd}.

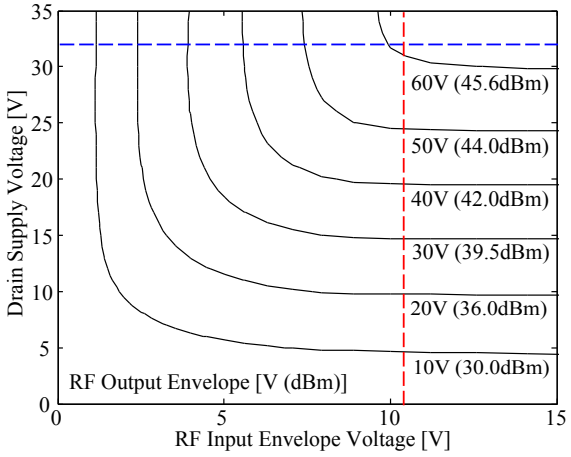
A rapid change in $|\tilde{v}_{out}|$ causes a rapid change in I_{dd}, requiring the DC supply to have low output impedance over the $|\tilde{v}_{out}|$ bandwidth (amplitude modulation bandwidth). Poor bias network design is a frequent cause of memory effects in drive-modulated PAs, in which PA gain changes in time due to the V_{dd} error incurred by finite output impedance.

Drain modulated systems require V_{dd} to vary quickly, and thus cannot tolerate the bank of capacitors. Any capacitance remaining at the V_{dd} node must be driven by the EM, reducing efficiency. Instead the EM must replace the capacitors, presenting a low output impedance over a broad frequency range.

The block diagram of the EM used in this work is shown in Fig. 3, and is of a similar concept to the circuit described in [8]. A wide-bandwidth linear amplifier controls the voltage V_{dd}, but is very inefficient. A high-efficiency switched mode power supply (SMPS) strives to minimize the current from the linear amplifier. This architecture demonstrates a clear tradeoff between efficiency (SMPS) and linearity (linear amplifier). An EM weighted toward efficiency will have reduced bandwidth, slew rate, and output impedance bandwidth, incurring some degree of V_{dd} distortion. Various approaches to addressing EM realization challenges have been reported in [9]–[13]. In the next section a method is presented to determine minimum performance required of the EM, allowing optimization of EM efficiency.

C. PA Characterization for ET Operation

A primary component of traditional PA characterization is an input power sweep with fixed V_{dd}. Operation in an ET system introduces V_{dd} variation, adding a new degree of freedom which must also be characterized using new methods (e.g. [15], [16]). Fig. 4(a) and (b) completely describe the performance of a GaN HEMT PA at 2.14 GHz for a range of RF input voltage levels ($|\tilde{v}_{in}|$) and drain voltage levels (V_{dd}), neglecting any time-variant change in PA behavior. The



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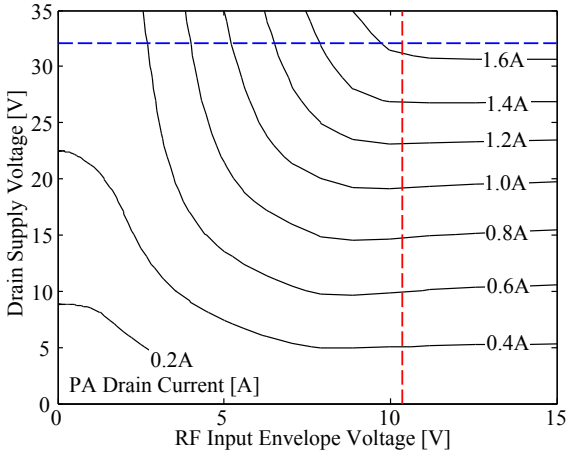


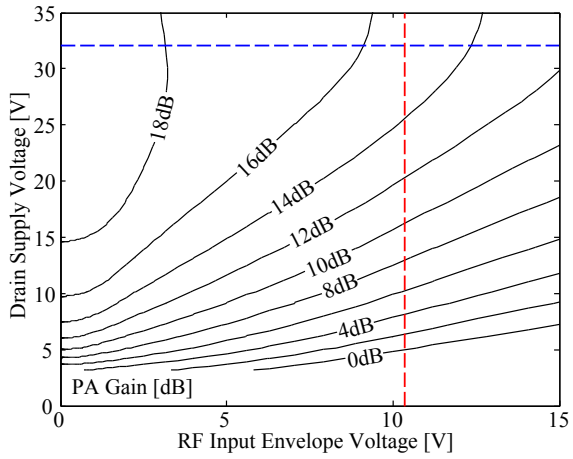
(b)

Fig. 4. Static behavioral model of a simulated PA over varying drain supply voltage and input power. The blue dashed line shows drive-modulated operation, while the red dashed line shows pure drain-modulated operation.

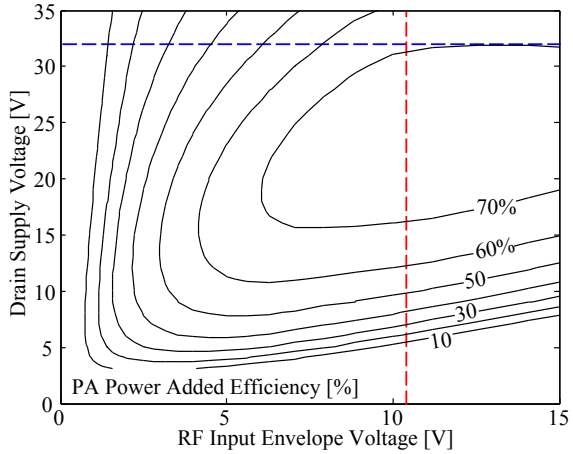
horizontal and vertical dashed lines in each figure illustrate drive-modulated and pure drain-modulated operation, two extremes in which output power is controlled exclusively by either $|\tilde{v}_{in}|$ or V_{dd} while the other is held constant. Under drive modulation the output power increases with input drive to a maximum value and then remains constant; the maximum possible output power achievable varies with V_{dd}. Under drain modulation output power increases quite linearly with V_{dd}, provided $|\tilde{v}_{in}|$ is large enough.

All of the metrics listed earlier in this section (gain, efficiency, drain resistance, etc.) can be derived from the dataset shown in Fig. 4. For example, Fig. 5 shows the PAE and gain of the PA at every possible ET operating point.

Under drive modulation gain decreases as the PA enters high-power, high-efficiency compressed operation, causing distortion of the output signal. If the gain variation is well-known and repeatable (static) the input signal can be "pre-distorted" to achieve the desired output (e.g. input power will be increased at high output power levels where PA gain is known to be low). Digital Pre-Distortion (DPD) techniques



(a)



(b)

Fig. 5. PAE and gain of the simulated PA over varying drain supply voltage and input power, derived from the PA characterization of Fig. 4.

derive and apply such corrections in the baseband domain.

Under pure drain modulation, efficiency remains high over a larger output power range. PA gain variation is much more significant in this case than under traditional drive modulation, requiring significant pre-correction of $\tilde{v}_{in}$. Errors in V_{dd} will cause the PA to have an unexpected value of gain and insertion phase which was not pre-corrected using DPD; V_{dd} distortion translates into transmitter output distortion.

We define drain sensitivity as a metric describing the transfer function $V_{dd} \rightarrow |\tilde{v}_{out}|$ where $|\tilde{v}_{out}|$ is a function of both V_{dd} and $|\tilde{v}_{in}|$:

$$S_{drain} = \frac{\partial |\tilde{v}_{out}|}{\partial V_{dd}} \cdot \frac{V_{dd}}{|\tilde{v}_{out}|} \cdot 100 \qquad (8)$$

S_{drain} indicates the ability of drain voltage to control output power, and is typically large in high-efficiency, gain-compressed PA operation. Drain sensitivity varies with PA operating point, as shown by the contours of Fig. 6. Under drive modulation S_{drain} remains low, except in gain compression. Under pure drain modulation the PA is always in gain compression, resulting in high S_{drain} over the whole output

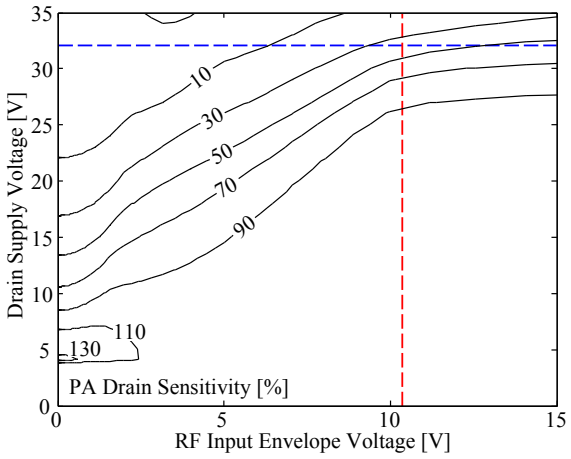


Fig. 6. Sensitivity of PA output amplitude to drain voltage variation ($V_{dd} \rightarrow |\tilde{v}_{out}|$) calculated using the metric of Eqn. 8 and the PA characterization of Fig. 4(a).

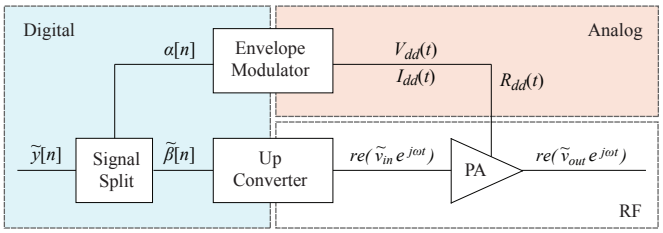


Fig. 7. General ET transmitter block diagram. The α and $\tilde{\beta}$ waveforms are derived from the desired signal $\tilde{y}$ such that the PA produces $\tilde{v}_{out}$ equal to $\tilde{y}$ (linear output), with high efficiency.

power range and indicating that drain voltage variation has a strong influence on output power. Therefore very precise control of V_{dd} is required to maintain transmitter linearity.

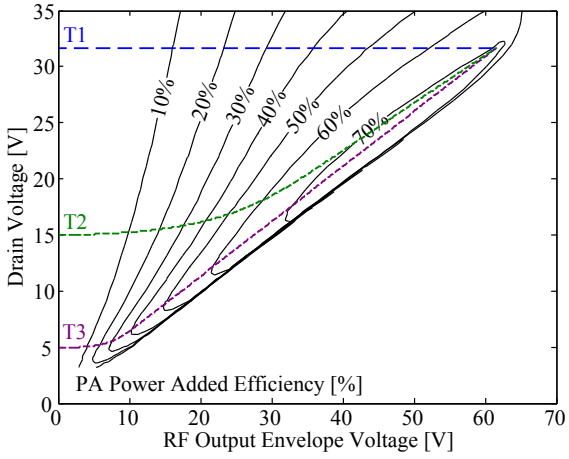
III. Envelope Tracking System Overview

Pure drain and drive modulation are unable to produce a wide range of $|\tilde{v}_{out}|$ with high efficiency. In the ET system described here, both V_{dd} and $|\tilde{v}_{in}|$ are varied simultaneously to achieve high PA efficiency over a wide output power range. A general ET transmitter block diagram is shown in Fig. 7.

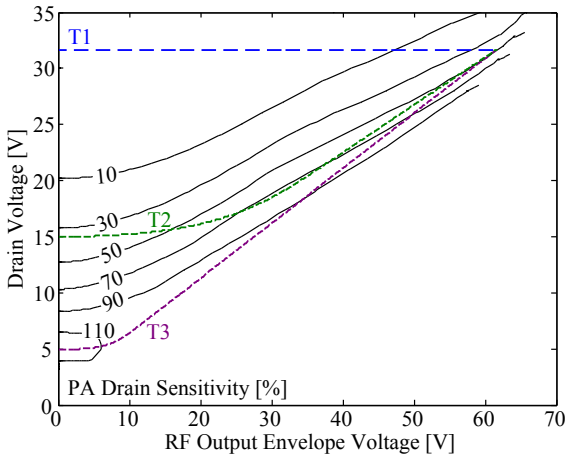
A. Signal Split Design

The "signal split" block applies a transformation to the desired signal envelope $|\tilde{y}|$ to produce the EM input α. An ideal EM produces V_{dd} equal to α; an EM optimized for efficiency produces V_{dd} which is a distorted version of α. The signal split block also pre-distorts the desired complex baseband signal $\tilde{y}$ to produce $\tilde{\beta}$, correcting for the expected variation of PA gain and insertion phase due to V_{dd} variation. An upconverter applies this modulation to an RF carrier, resulting in the modulated PA input signal $\Re(\tilde{v}_{in}e^{jwt})$.

The ratio of drain and drive modulation is selected at each output amplitude to meet two system-level goals: efficiency and linearity. The tradeoff is clearly seen by re-plotting the PA characterization data using $|\tilde{v}_{out}|$ as the independent variable

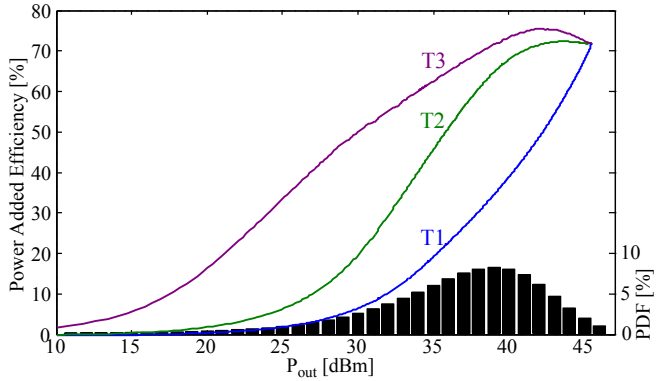


(a)



(b)

Fig. 8. PAE and drain sensitivity, plotted versus $|\tilde{v}_{out}|$. Three operating trajectories are shown which could be used to determine the relationship between V_{dd} and $|\tilde{v}_{out}|$, each implemented as a different "signal split" in the block diagram of Fig. 7.



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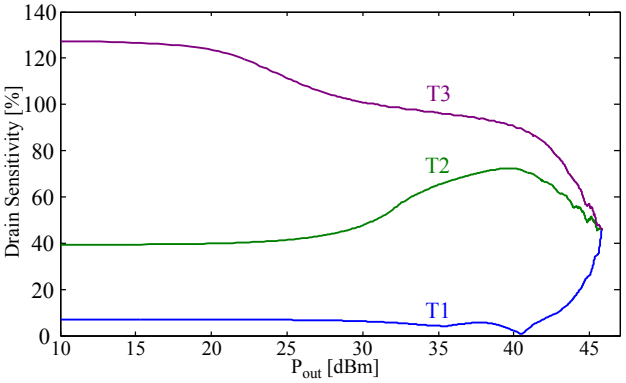


(b)

Fig. 9. PAE (a) and S_{drain} (b) vs. output power for three different V_{dd}-$|\tilde{v}_{in}|$ trajectories. Probability density function of a 7 dB PAR W-CDMA downlink signal is shown by the histogram in (a).

as shown in Fig. 8 for PAE and S_{drain}. Three operating trajectories (signal splits) are shown (T1, T2, and T3) which could be used to determine the relationship between V_{dd} and $|\tilde{v}_{out}|$. For comparison, trajectory T1 implements traditional drive modulation, where V_{dd} remains constant.

B. PA Performance

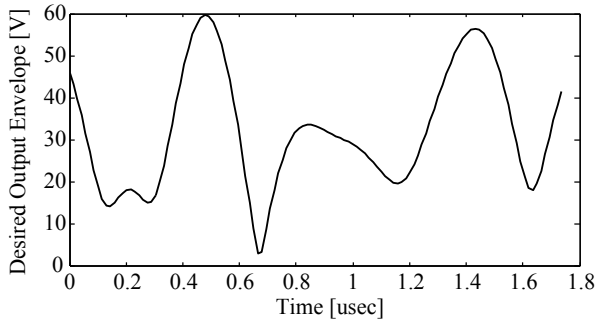
Each trajectory results in a different PA efficiency characteristics over output power and requires a different degree of precision in the V_{dd} waveform. These trends are shown by the plots of Fig. 9. The resulting PA performance assuming a W-CDMA downlink modulation at 7 dB PAR is shown in Table. I. Trajectories T2 and T3 achieve increased PA efficiency also have high sensitivity to V_{dd} errors (as shown in Fig. 8(b)), requiring the EM to produce the required waveform more precisely. The high-efficiency trajectories also require larger voltage slews, higher-bandwidth voltage and current variation variation, and larger voltage range.

To further illustrate the impact on EM requirements a short segment of a the W-CDMA waveform envelope amplitude is shown in Fig. 10(a) along with the resulting V_{dd}, R_{dd}, and S_{drain} waveforms for each trajectory.

There is no general relationship between the bandwidth of a complex baseband signal and the bandwidth of its amplitude because the transformation between the two is nonlinear. As an example, consider that GSM waveforms have no power variation and thus zero envelope bandwidth, but the W-CDMA waveform has envelope bandwidth many times larger than that of the complex modulation. Furthermore, each trajectory of Fig. 8 transforms the original envelope (Fig. 10(a)) into a V_{dd} waveform (Fig. 10(b)) with different dynamic range and bandwidth content. The trajectory selected also dramatically impacts the drain resistance waveform (Fig. 10(c)): ranging from smooth variation (T1) to very fast load variation (T3).

TABLE I
PA PERFORMANCE FOR T1, T2, AND T3

Trajectory	PA PAE	PA Gain
T1	33 %	17.3 dB
T2	60 %	15.9 dB
T3	71 %	13.8 dB



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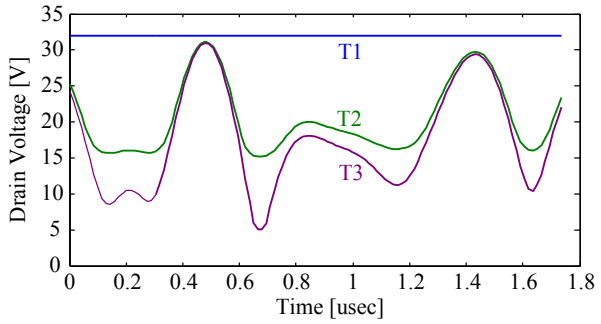

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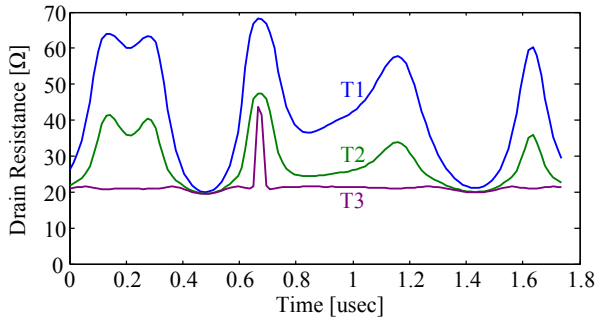
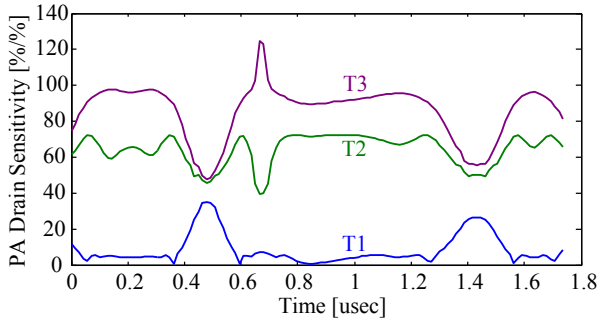


(c)



(d)

Fig. 10. PAE and sensitivity of the PA output amplitude to drain voltage variation, plotted vs. output amplitude. Three operating trajectories are considered. Each results in a different average PA efficiency and requires a different degree of precision in the V_{dd} waveform.

C. Envelope Modulator Linearity Requirements

An envelope modulator must be optimized for efficiency while maintaining performance sufficient to meet system linearity requirements. Unfortunately the relationship between EM distortion and system linearity degradation is very complex, depending upon:

- PA drain sensitivity when the distortion occurs;
- spectral power and frequency of the distortion; and
- amplitude level of the distortion.

A method is described in [17] to analyze the impact of EM distortion on system linearity, establishing component-level EM requirements. The same analysis method is used here to show the consequences of PA and system decisions on EM requirements.

The simulation generates α from a 7 dB PAR downlink W-CDMA signal and computes the pre-corrected $\tilde{\beta}$ waveform using the PA characterization data of Fig. 4. Bandwidth and rate limit non-idealities are applied to the α to produce V_{dd}, emulating two common types of non-ideal EM behavior. Finally, V_{dd} and $\tilde{v}_{in}$ are re-combined using the PA characterization data to produce $\tilde{v}_{out}$.

Linearity is evaluated using adjacent channel power (ACP), a transmitter linearity measure calculated as the ratio of power produced in a neighboring channel to the in-band power produced. ACP is limited to -45 dBc for W-CDMA downlink transmitters by 3GPP specifications [18], and -65 dBc represents a negligible contribution to system distortion. The simulation is limited by numerical accuracy to -77 dBc. For the EM bandwidth and slew rate shown in Table II the EM contributes a negligible amount of ET transmitter distortion (-65 dBc ACP). Simulation results clearly show the inter-dependence of PA behavior, system-level design, and EM requirements: the system increases PA efficiency at the expense of PA drain sensitivity, requiring a more precise EM design, which is likely to have reduced efficiency.

The tool described in [17] is also useful for synthesizing input V_{dd} waveforms and I_{dd} loading waveforms for EM circuit-level simulations. The output of such circuit simulations can be passed back to the tool to project the contribution of more complex EM distortion mechanisms to system distortion.

IV. ET System Results

A test bed has been assembled using commercial test and measurement equipment for signal generation, upconversion, and acquisition. MATLAB was used for instrument control and to implement several signal processing and equipment automation. The 40-W class-F^{-1} PA prototype characterized in Fig. 1 was integrated with an EM prototype and linearized using the ET test bed. The $V_{dd} - \tilde{v}_{in}$ trajectory selected was

TABLE II
EM Requirements to Achieve Negligible ET System Distortion

Trajectory	Min. EM Bandwidth	Min. EM Slew Rate	Min./Mean/Max. V_{dd}
T1	0 MHz	0 V/μsec	32.0 V / 32.0 V / 32.0 V
T2	17 MHz	150 V/μsec	15.0 V / 18.3 V / 32.0 V
T3	23 MHz	230 V/μsec	5.0 V / 15.0 V / 32.0 V

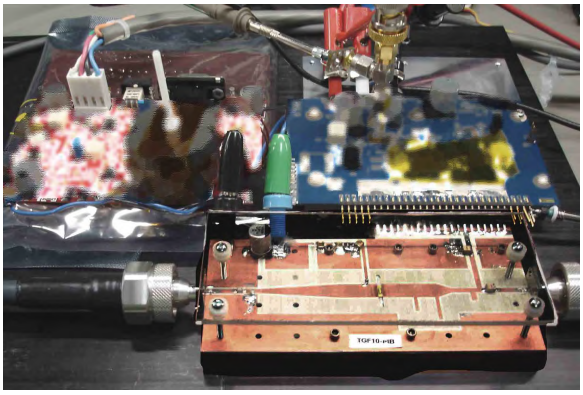


Fig. 11. Proof-of-concept envelope tracking system hardware.

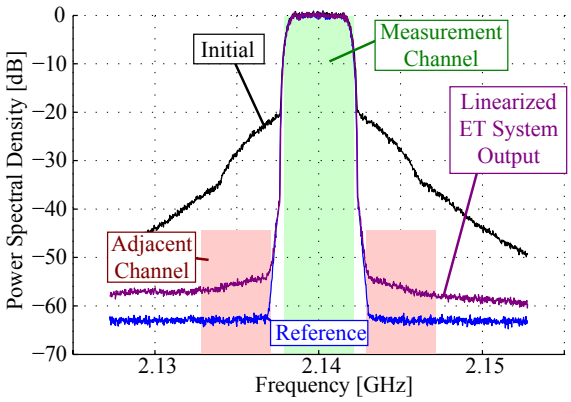


Fig. 12. Measured RF output spectra for the proof-of-concept system before and after linearization steps. A reference trace indicates the measurement noise floor.

most similar to T3 (shown in Fig. 8). Prototype hardware is shown in Fig. 11.

In addition to the DPD correction several other linearization steps were developed and implemented to address transmitter distortion due to other parts of the system:

- a path time-alignment algorithm precisely synchronizes the V_{dd} and $\tilde{v}_{in}$ waveforms at the PA,
- an EM frequency response equalization extends the flat-gain bandwidth, and
- adaptive polynomial-based DPD [19] rejects PA memory effects and residual system distortion.

Measured initial and corrected RF output spectra are shown in Fig. 12 and compared to a reference measurement. ACP performance of the final ET system exceeds 3GPP requirements by 10 dB at 5 MHz. Further details of this hardware and algorithm implementation are discussed in [20].

Table III shows power and efficiency results comparing ET operation to drive-modulated operation. The same PA and 7 dB PAR W-CDMA downlink modulation was used for both tests. Both systems use linearization techniques to exceed linearity requirements, and both achieve the same output power. However, the ET system operates much more efficiently than drive modulation, improving system drain efficiency from 30 % to over 50 %. Operating from a battery the ET system would last 75 % longer, and in a fixed installation the ET system consumes 43 % less power.

Power dissipation is reduced and also spread among two components. PA dissipation is reduced from 19.8 W to only 2.7 W, reducing the system's cooling requirements.

TABLE III
TRANSMITTER PERFORMANCE MEASUREMENTS FOR TRADITIONAL AND ET CONFIGURATIONS USING A HIGH-EFFICIENCY CLASS-F^{-1} PA

	Drive Modulation	Envelope Tracking
ACP at 5 MHz	-57.0 dBc	-55.7 dBc
ACP at 10 MHz	-58.3 dBc	-57.8 dBc
Average RF Output Power	8.5 W	8.5 W
Peak RF Output Power	40.0 W	40.0 W
Transmitter Drain Efficiency	30.0%	52.5%
Transmitter Supply Power	28.3 W	16.2 W
Transmitter Dissipated Power	19.8 W	7.7 W
EM Efficiency	–	69.1%
EM Input Power	–	16.2 W
EM Dissipated Power	–	5.0 W
PA Drain Efficiency	30.0%	75.9%
PA Drain Supply Power	28.3 W	11.2 W
PA Dissipated Power	19.8 W	2.7 W

V. CONCLUSION

This paper presents an overview of the envelope tracking RF transmitters which require a dynamic power supply implemented as an envelope modulator. Specifically, we address design of transmitters for wireless communications at the base station in the 2.14 GHz band with W-CDMA modulation. A new approach to PA characterization and a system modeling method are developed to determine envelope modulator requirements. System measurements of a proof-of-concept ET system achieves more than 50 % system PAE.

An understanding of PA behavior provides insight into the type of drain voltage waveform required to improve its efficiency, and also the drain current waveform that will be required. Section 2 presents representative PA characteristics, but it must be noted that PA behavior varies widely with design objectives - not all PAs will perform equally well in an ET system. [21] suggests specific methods of optimizing PA design for ET operation. Sections 3 and 4 demonstrated the impact of system V_{dd}-$\tilde{v}_{in}$ trajectory on PA performance and EM requirements, emphasizing the importance of close collaboration and co-design of PA and EM components.

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