Envelope Tracking Transmitter System Analysis Method

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***Abstract*— A general envelope tracking (ET) transmitter is described which utilizes both drive and drain modulation. We develop a simulation method useful for modeling the impact of component non-idealities on system performance, starting from hardware measurement data. An example analysis evaluates tradeoffs between ET system linearity, power amplifier efficiency, and envelope modulator requirements for a W-CDMA down-link transmitter.**

I. Introduction

The final stage power amplifier (PA) is typically the largest contributor to transmitter inefficiency. Fig. 1 shows the measured power-added efficiency (PAE) vs. output power for a GaN HEMT class-AB PA. The average efficiency depends on signal modulation. The envelope amplitude PDF of a de-crested single-carrier W-CDMA down-link signal is shown in Fig. 1 to illustrate this point. For a constant 32-V drain supply voltage the PA produces infrequently-occurring peak output power (50 dBm) with high efficiency of 65%. The average output power of 42 dBm, produced with only 20% PAE will be the largest contributor to the average modulated efficiency.

PAE improvement over a wide range of output power levels can be achieved using ET transmitters [1]. In this case a drain bias control circuit (envelope modulator, or EM) varies the drain supply voltage (v_{dd}) to dynamically adjust the operating point of the microwave transistor. An ET transmitter optimized for PA efficiency varies v_{dd} to operate the transistor along the dashed line in Fig. 1 with 50% efficiency at the average output power level. However, the PA is not the only component in an ET transmitter, and highest PA efficiency does not necessarily translate to highest transmitter efficiency.

One possible implementation of an ET transmitter is shown in Fig. 2 with the following signal flow:

- $\tilde{y}[n]$ (desired digital baseband signal) is digitally pre-distorted to compensate for ET system dynamic nonlinear effects;
- $\tilde{x}[n]$ is split into a real valued component $\alpha[n]$, and a complex valued component $\tilde{\beta}[n]$;
- $\alpha[n]$ varies the PA drain supply voltage $v_{dd}(t)$ at the rate of the signal envelope through the EM;
- $\tilde{\beta}[n]$ is delayed and up-converted to RF through an IQ modulator to form the PA input RF signal $v_{in}(t)$;
- $v_{out}(t)$ is produced by non-linear combination of $v_{in}(t)$ and $v_{dd}(t)$ in the PA, ideally equal to $\tilde{y}[n]$;
- $\tilde{z}[n]$ is a down-converted, digitized version of $v_{out}(t)$ used to adapt the DPD, signal split, and delay.

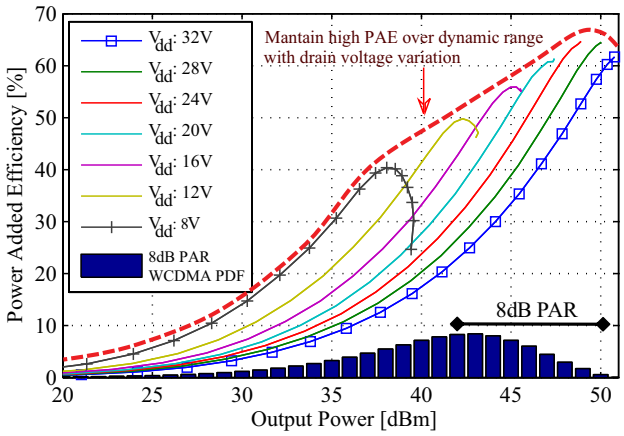


Fig. 1. Measured efficiency vs. output power for varying drain voltage for a class-AB PA prototype using a Nitronex 25100 GaN HEMT transistor. W-CDMA single-carrier down-link waveform PDF bar plot included below. The signal has been de-crested to set average power 8 dB below peak power.

The transfer functions of the analog/RF components in Fig. 2 are non-ideal due to frequency dependence, phase imbalance, quantization error, and path delay differences between v_{dd} and v_{in}, to name a few. The design of the digital blocks (DPD, signal split, adaptive delay) must take into account the non-idealities of the analog/RF components. This paper describes a method that can be used to quantify the impact of component non-idealities and inter-dependency on the overall ET transmitter linearity ($\tilde{y} \rightarrow \tilde{z}$) and efficiency ($\eta_{ET} = \eta_{EM} \times \eta_{PA}$). The method is also useful for design, simulation, and optimization of algorithms by emulating ideal or non-ideal hardware. The method is applied to evaluation of PA efficiency vs. EM requirements for an ET transmitter system described in the next section.

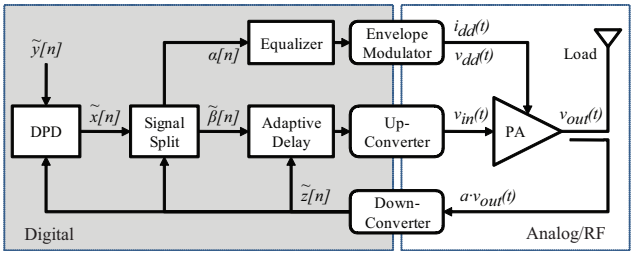


Fig. 2. One possible block diagram of an ET transmitter system.

II. ET System and Components

The topology in Fig. 2 differs from those presented in the literature (e.g. [1]), but the analysis method presented here applies generally. The relevant aspects of each component are discussed below.

A. Power Amplifier

In an ET transmitter the PA acts as a nonlinear combiner of v_{in} and v_{dd}, and the output signal (v_{out} into a 50Ω load) is a strong function of both inputs. Unlike purely drive- or drain-modulated transmitters, the output signal linearity is therefore critically dependent upon the linearity of both v_{dd} and v_{in} paths.

A given output power can be produced using a wide range of RF input envelope amplitude (denoted $|v_{in}|$) and v_{dd} combinations, each resulting in a different level of PA saturation. PA efficiency, required drain supply current (i_{dd}), and PA insertion gain and phase also vary depending on the proportions of v_{dd} and v_{in}. The PA can be characterized over v_{dd} and $|v_{in}|$ domain using various techniques, some of which are discussed in literature (e.g. [2], [3]), resulting in plots such as the one shown in Fig. 3. In ET simulations this data set will be used as a static 2-d look-up table model for PA behavior.

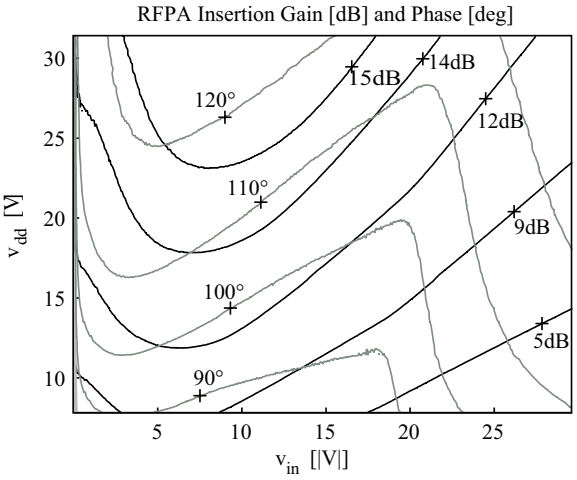
For example, if at an instant in time the $|v_{in}|$ and v_{dd} are 15 V and 25 V respectively the PA insertion gain and phase will be 14 dB and 110 degrees while PA efficiency and drain current will be 58 % and 4.2 A.

This static measurement method reflects PA behavior under pulsed operating conditions faster than the thermal time constant of the device. Therefore dynamics due to thermal loading, charge storage, etc. are isolated from static behavior, leading to a memoryless PA model. In this way only ET system dynamics can be analyzed separately from PA dynamics. In an ET transmitter PA dynamics are dealt with using standard pre-distortion methods (e.g. [4]) implemented in the DPD block of Fig. 2.

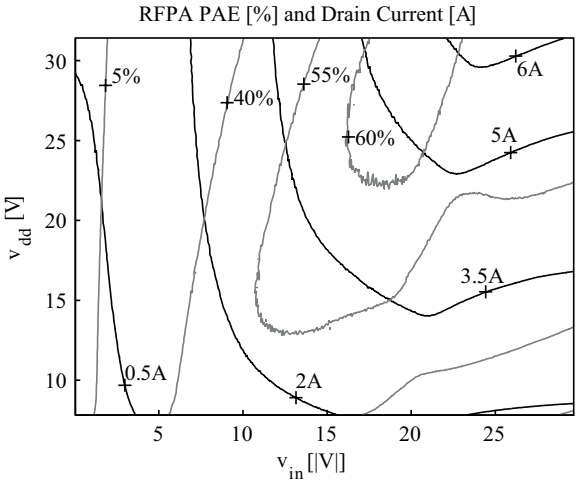
B. Signal Split

Classical envelope elimination and restoration (EER) systems set the v_{dd} equal to the signal envelope amplitude, sacrificing system linearity, EM efficiency, and PA gain at the lower envelope power levels. In Fig. 4(a) the gradient shows PA efficiency for all possible v_{dd} / $|v_{out}|$ combinations. Three v_{dd} trajectories, denoted T1, T2, and T3, achieve different modulated PA efficiencies as summarized in Table 1. For example, T1 has lower minimum voltage and larger first derivative, presenting a challenge to the EM which must produce higher bandwidth voltage waveforms over a wider voltage dynamic range. The signal split block of Fig. 2 digitally transforms $\tilde{x}$ into α from which the EM produces the required v_{dd}.

Fig. 4(a) shows required PA insertion gain and phase variation for each trajectory. These curves are digitally



(a)



(b)

Fig. 3. Measured PA insertion gain, phase, (a), and drain current, PAE (b), over all ET operating conditions. Very low average output power (high-PAR) waveforms are used to avoid thermal interaction.

implemented by the signal split as a transfer function $\tilde{x} \rightarrow \tilde{\beta}$ to produce a v_{in} which restores system linearity. This transformation is analogous to the memoryless pre-distortion used in [1]. Fig. 4(b) also shows the change in PA drain resistance (EM load resistance) for each trajectory. T1 is associated with the largest first derivative of the drain resistance, and thus the most difficult dynamic load regulation challenge to the EM.

C. Envelope Modulator

Error in the EM output waveform v_{dd} will cause uncompensated variation in the PA output v_{out} and result in ET system distortion. The EM design task is a compromise among many characteristics including small signal bandwidth, large signal slew rate, voltage range, load regulation, and efficiency. These requirements impact the

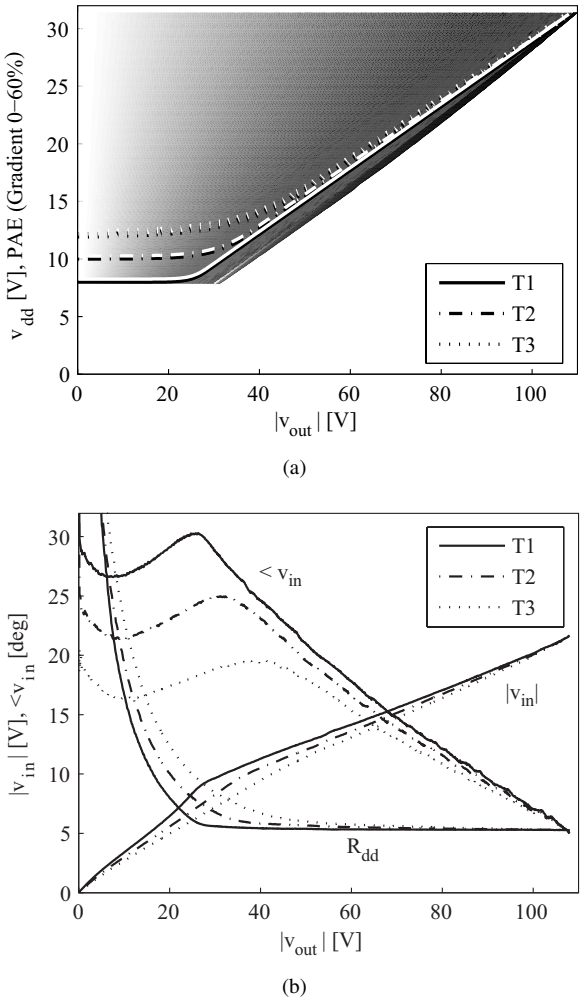


Fig. 4. (a) Three possible signal split trajectories result in varied PA modulated efficiency. The gradient indicates PA efficiency ranging from 0 % to 60 %. (b) PA input signal gain and phase adjustment required to account for drain voltage variation. Drain resistance is also shown at each output voltage level.

following:

- ET system efficiency is roughly defined as $\eta_{ET} = \eta_{EM} \times \eta_{PA}$, demanding high EM efficiency;
- High η_{PA} requires large voltage and current operation, reducing η_{EM};
- Inadequate bandwidth, slew rate, or load regulation will translate through the PA into v_{out} distortion and degrade system linearity.

The EM is commonly implemented as an efficient low-bandwidth switched-mode power supply (SMPS) working in concert with a high-bandwidth but inefficient linear amplifier [5]. Increasing bandwidth and slew rate requirements forces the high-bandwidth linear amplifier to produce a larger portion of the output power, reducing EM efficiency. Accurately predicting EM efficiency using the previously mentioned EM requirements is a complicated task and lies outside the scope of this paper.

D. Digital Signal Processing

The DPD, signal split, and adaptive delay algorithms of Fig. 2 are designed to compensate non-linearity and dynamic effects adaptively with changing operating conditions. The simulation method described in the next section serves as a test-bed for algorithm development and optimization. In a finished implementation of the ET transmitter these algorithms must be optimized with non-ideal hardware, finite dynamic range and sample rate, and limited computational complexity.

III. System Analysis Tool

Each of the components in the previous section has been implemented in a Matlab simulation environment using the block diagram of Fig. 2. A standard W-CDMA downlink signal is generated at a 20x oversampling rate, and de-crested to 8 dB PAR ($\tilde{y}[n]$). DPD can be applied at this stage, resulting in $\tilde{x}[n]$. This is followed by the signal split which produces $\alpha[n]$ and $\tilde{\beta}[n]$ according to one of the trajectories shown in Fig. 4(a). EM and up-converter models translate $\alpha[n]$ and $\tilde{\beta}[n]$ into $v_{dd}(t)$, and $v_{in}(t)$. The PA is modeled using the 2-d look-up table formed by the data of Fig. 3. A variety of non-idealities are synthesized to distort the $v_{dd}(t)$, $v_{in}(t)$, and $\tilde{z}[n]$. A few examples include DAC quantization, up-converter phase imbalance, EM group delay, PA thermal memory effect, and ADC path frequency response. The impact of component non-ideality on system efficiency, linearity, and on the performance of other components can thus be easily observed.

A generic EM was modeled using the cascade of a low-pass filter a slew-rate limiter (two key limitations in EM design directly opposing to ET efficiency). The ideal $v_{dd}(t)$ signal component was distorted by this EM model for a variety of EM bandwidth and EM slew rate limitations and then recombined with the $v_{in}(t)$ signal using the PA model. The $v_{out}(t)$ signal linearity was then evaluated using error vector magnitude (EVM) and adjacent channel power (ACP). ACP was found to be the limiting metric. Fig. 5 shows degradation in ET system linearity due exclusively to EM non-ideality.

As mentioned in the previous section, increased PA efficiency can be achieved with an aggressive signal split at the expense of increased EM requirements. The method described above was used to quantify EM bandwidth and slew rate performance required to achieve ET system linearity of -45 dBc ACP and -65 dBc ACP (in which the EM has a nearly negligible system linearity impact) with the three signal split trajectories shown in Fig. 4(a). The simulation noise floor due to quantization, interpolation, and numerical accuracy was less than -69 dBc ACP.

Fig. 6 summarizes the resulting EM requirements for each signal split trajectory, drawing a clear connection

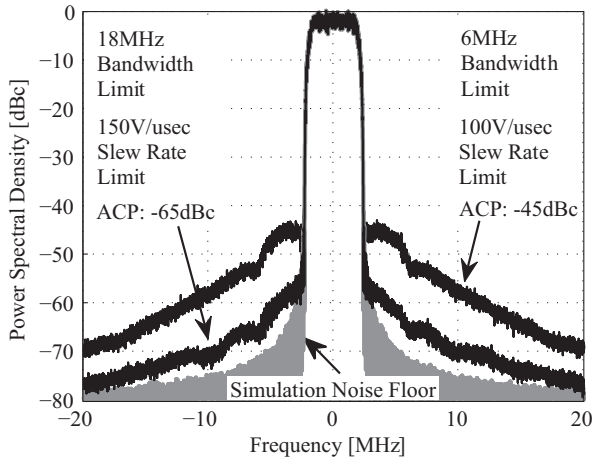


Fig. 5. Simulated ET system output power spectral density for a 1-carrier W-CDMA waveform using trajectory T2 from Fig. 4(a) given two EM models. Degradation in ACP is due only to EM non-ideality. The system noise floor shown in gray.

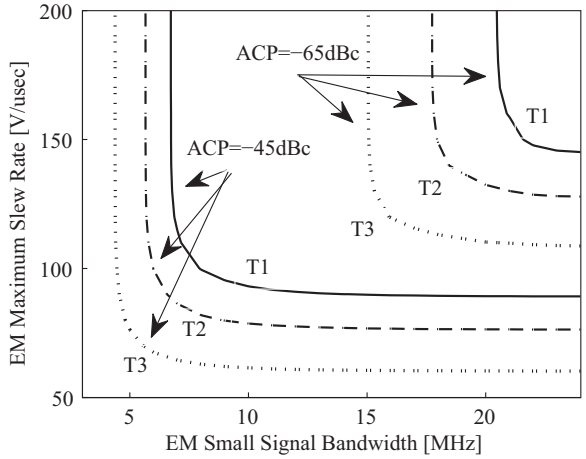


Fig. 6. EM bandwidth and slew rate required to meet -45dBc (3GPP minimum spec) and -65dBc adjacent channel power considering only distortion from the v_{dd} path for each of the signal split trajectories shown in Fig. 4(a).

between EM component behavior and ET system performance. From a system design perspective we see that signal splits weighted toward high PA efficiency clearly require higher EM bandwidth, slew rate, and voltage dynamic range (all of which lead to reduced EM efficiency). Summarized in Table I, these results give the EM and system designers a starting point for designs and insight into system-level tradeoffs.

The DSP algorithms of Fig. 2 are initially designed using ideal models. This simulation method allows us to re-introduce previously mentioned non-idealities one at a time, observe the impact on system performance, and modify the algorithm. DSP block parameters can then be optimized, e.g. number of bits, update rates, and

TABLE I
SIMULATED ET SYSTEM COMPONENT TRADES

Signal Split	PA PAE	Min./Mean/Max. V_{dd}	Min. EM Bandwidth	Min. EM Slew Rate
T1	50.6 %	8.0 V / 11.0 V / 31.5 V	20 MHz	150 V/usec
T2	47.5 %	10.0 V / 12.3 V / 31.5 V	18 MHz	130 V/usec
T3	43.4 %	12.0 V / 14.0 V / 31.5 V	15 MHz	110 V/usec

degree of complexity, to reduce processing and memory requirements while maintaining system performance.

IV. CONCLUSION

In summary, this paper presents a useful method for translating component behavior into system performance metrics. PA dynamics (memory effect behavior) are separated, allowing a clear distinction between ET- and PA-induced distortion not possible in hardware. The general steps for the analysis method are:

- Measure or simulate the PA to obtain data of Fig. 3;
- Plot possible signal split trajectories and determine impact on PA performance as in Fig. 4 and Table I;
- Simulate system performance for each trajectory using either a generic or circuit model for the EM;
- Choose optimal trajectory for best system efficiency and design/optimize DSP algorithms.

A wide variety of analyses are possible using this general method. The ability to consider only one type of non-ideality in an otherwise perfect ET system proves advantageous in development of efficient and linear ET transmitters.

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REFERENCES

[1] D. Kimball, J. Jeong, C. Hsia, P. Draxler, S. Lanfranco, W. Nagy, K. Linthicum, L. Larson, and P. Asbeck, "High-efficiency envelope-tracking w-cdma base-station amplifier using gan hfets," *IEEE Trans. Microwave Theory Tech.*, vol. 54, no. 11, pp. 3848–3856, Nov. 2006.

[2] H. Nemati, C. Fager, U. Gustavsson, R. Jos, and H. Zirath, "Characterization of switched mode ldmos and gan power amplifiers for optimal use in polar transmitter architectures," in *2008 IEEE MTT-s Dig.*, June 2008, pp. 1505–1508.

[3] J. Hoversten, M. Norris, Z. Popovic, and D. Maksimovic, "Optimal pae polar split for efficient and linear drain modulated power amplifiers," in *2009 IEEE Topical Workshop on Power Amplifiers for Wireless Communications*, Orlando, FL, Jan. 2009.

[4] A. Zhu, P. Draxler, J. Yan, T. Brazil, D. Kimball, and P. Asbeck, "Open-loop digital predistorter for rf power amplifiers using dynamic deviation reduction-based volterra series," *IEEE Trans. Microwave Theory Tech.*, vol. 56, no. 7, pp. 1524–1534, July 2008.

[5] V. Yousefzadeh and et. al., "A digitally controlled dc/dc converter for an rf power amplifier," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 164–172, Jan. 2006.