GaN HEMT PA with over 84% power added efficiency

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Described are the design procedure and measured performance of a PA targeted for the W-CDMA downlink band exhibiting over 84% PAE at 2.14 GHz. The PA is designed with an uncharacterised GaN HEMT. A measurement-based design approach is used to optimise the source and load impedance at the fundamental frequency with class- F^{-1} harmonic terminations enforced. *S*-parameters extracted from a full-wave EM model characterising the impedance transformation from the virtual drain of the GaN HEMT to an output matching circuit are used to design class-F^{-1} second- and third-harmonic terminations. The highest efficiency for the final PA occurred 10 MHz off the design frequency, exhibiting 84.9% PAE, 8.2 W output power and 18.4 dB of gain at 2.15 GHz.

Introduction: New GaN technology provides microwave PA designers with high frequency, high power transistors having low parasitics [1]. Recently-introduced transistors often lack a nonlinear model suitable for efficient PA design, or an existing nonlinear model fails to accurately reproduce measured performance in high efficiency operation points near the I–V axes. This usually means that several design iterations are required in order to realise an efficient PA. Alternatively, a measurement-based design technique involving source pull and load pull may be adopted [2].

Class-F and class-E PAs having greater than 80% PAE and over 5 W output power near 2 GHz have been reported [3, 4]. This Letter details the measurement based design of a class-F^{-1} PA at a centre frequency of 2.14 GHz. The PA exhibits 7 W output power and 84.6% PAE with a drain voltage of 31 V at 2.14 GHz. A 0.69 dB improvement in output power and 84.9% PAE was obtained at 2.15 GHz. Full-wave EM modelling of the die-to-matching-network transition was used in order to accurately determine the $2f_0$ and $3f_0$ impedances at the virtual drain. Input and output pre-match circuits were designed and class-F^{-1} harmonic traps were verified. Fundamental frequency source and load pull with class-F^{-1} harmonic terminations were performed to determine optimal fundamental frequency source Z_S and load Z_L impedance. Finally, the prototype PA was designed with integrated bias lines. The straightforward design procedure resulted in a first-pass success, yielding an efficient PA using an unmodelled device.

Fundamental load pull with class-F^{-1} harmonic terminations: The device under test (DUT) was the Triquint TGF2023-02 12 W bare die power GaN on SiC, which operates up to 18 GHz [5]. A 0.68 pF output capacitance (C_{out}) was calculated using the linear model provided in the device datasheet. The low C_{out} of the device coupled with significant gain at multiple harmonics of 2.14 GHz makes this device an excellent candidate for a high efficiency PA design. A full-wave EM model of the transition model indicated in Fig. 1 was developed in Ansoft's HFSS to model the impedance transformation owing to the fringing capacitance from the die to the ground plane, as well as the impact of the two bond wires connecting the die to the microstrip [2]. The two-port *S*-parameters from plane P_1 to P_2 were calculated by cascading the *S*-parameters of the ideal C_{out} with the *S*-parameters of the transition model exported from HFSS.

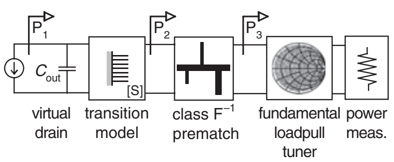

Fig. 1 *Load pull block diagram with defined reference planes for impedances*

Using the impedance transformation model, a microstrip pre-match was designed on a 30 mil Rodgers 4350B substrate. The load pre-match was designed to present the ideal class-F^{-1} $2f_0$ and $3f_0$ terminations at plane P_1 shown in Fig. 1. A source pre-match was designed without any specific input harmonic terminations. The *S*-parameters of the pre-match circuits were measured using modular fixtures as mentioned in [6] to verify the harmonic terminations of the output pre-match and calibrate the load pull measurements. The DUT bias current was set to approximately 50 mA with a drain voltage of 30 V. An initial approximation to the optimal Z_S of 3.1 $+j$13.8 Ω was determined by performing a small-signal fundamental frequency source pull for gain using a single slug tuner from FOCUS Microwaves. Z_S is referenced to the bonding plane on the input pre-match. It was found that the initial Z_S did not change for drain voltages between 25 and 35 V.

Large signal load pulls were performed to determine the optimal Z_L having maximum PAE, with at least 5 W output power. For each fundamental impedance point, a small input power sweep was performed to find the input drive level resulting in maximum PAE. An optimal Z_L of 164.5–j4.5 Ω was determined for a drain voltage of 30 V resulting in a PAE of 84.2%.

A final large signal source pull was performed to refine the source impedance, resulting in an optimal Z_S of 1.5 + j10.4 Ω, resulting in a PAE of 85.7%.

Prototype PA and measured performance: The prototype PA is shown in Fig. 2. The circuit was fabricated using an LPKF S62 milling machine. The input matching section was realised with parallel open circuit shunt stubs (OCSS) to present the low Z_S while reducing insertion loss. The output matching section used λ/4 OCSSs to present open and short circuits at $2f_0$ and $3f_0$, respectively. An additional OCSS is used to match the fundamental Z_L. American Technical Ceramics 100B and 600S capacitors were used for the DC block and bias line resonant capacitors, respectively. The microstrip ground plane is sweat soldered to a copper block, which serves as both a heatsink and continuous ground plane.

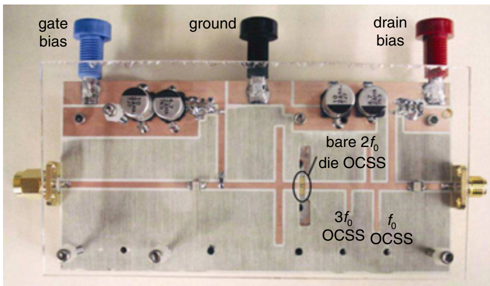

Fig. 2 *Photo of prototype amplifier measured for this Letter*

The PA exhibited over 80% PAE at V_{DD} = 30 V for a wide range of drain currents (50–200 mA). The best balance of PAE, output power and gain performance was measured using a drain current of 170 mA at 30 V, therefore all subsequent measurements were taken at this corresponding gate bias point. Measurements of the prototype PA performance at 2.14 GHz against input power are shown in Fig. 3 for the design point drain voltage of 30 V. The nonlinearity of the amplifier is evident by investigation of the gain against input power. The peak 2.14 GHz PAE is achieved under 3.6 dB gain compression.

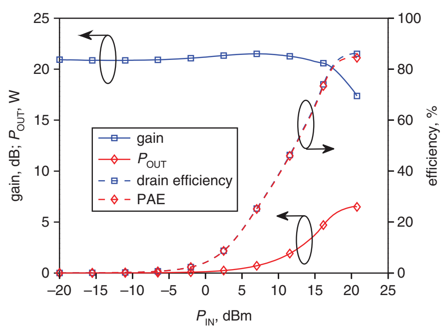

Fig. 3 *Measured PA performance at 2.14 GHz against input power, V_{DD} = 30 V*

The performance of the PA over the 2.10–2.18 GHz bandwidth is shown in Fig. 4 for a supply voltage of 34 V (chosen to show the peak measured PAE operating point). The PA exhibited its peak PAE of 84.9% at 2.15 GHz while maintaining over 70% PAE from 2.11–2.17 GHz. The significant reduction in PAE realised as the frequency departs from 2.14 GHz is expected, owing to the narrowband harmonic terminations presented by the OCSSs. An output power level between

7.7 and 8.4 W was maintained, while the gain exceeded 16 dB across the bandwidth, peaking at 19.3 dB at 2.13 GHz.

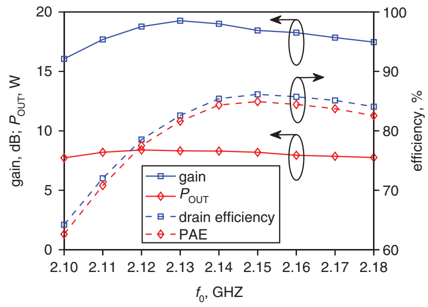

Fig. 4 *Measured gain, output power and efficiency against frequency at* $V_{DD} = 34$ *V*

Conclusions: A high efficiency PA design using an uncharacterised GaN HEMT is presented. While the design procedure was applied to a class-F^{-1} PA, the method is equally valid for other harmonically terminated high efficiency classes, such as class-F or class-E. Additionally, the technique is equally valid for other device technologies, such as an LDMOS device. This Letter demonstrates that development of a high efficiency, harmonically terminated PA without a model is both feasible and relatively straightforward.

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One or more of the Figures in this Letter are available in colour online.

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