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Custom IC for Ultra-low Power RF Energy Scavenging

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***Abstract*— This paper presents a custom IC that provides an efficient interface between an ultra-low power RF rectifying antenna (rectenna) power source and a microbattery for maximum power scavenging. The energy scavenger IC operates a boost converter in pulsed fixed-frequency discontinuous conduction mode to present a positive resistance to the rectenna. It uses current-starved circuitry, a non-overlapping gate-drive, and a sub-threshold current source to achieve a nominal supply current in the 200 nA range for V_{DD} = 2.5 V. Experimental results are given with the IC scavenging energy from a 1.93 GHz patch rectenna to a battery with voltages ranging from 2.5 V to 4.15 V. Overall conversion efficiency including all control losses is demonstrated at over 35 % at an input power of just 1.5 µW and at over 70 % at input power levels over 30 µW. The IC is fabricated in a 5 V, 0.35 µm CMOS process. Although the IC was designed for RF energy scavenging, the low power boost converter can be applied to other power sources such as wind, vibration, and temperature.**

***Index Terms* –** resistor emulation, RF energy scavenging, ultra-low power, DC-DC

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I. INTRODUCTION

As wireless sensor networks become more pervasive and sensor nodes operate at lower average power levels and are distributed in more remote and hazardous environments, the need to effectively and conveniently provide power to them becomes apparent. Energy scavenging can improve the functionality and performance of wireless sensors and devices by allowing them to operate with low maintenance for extended periods of time and by enabling further sensor miniaturization [1].

Controlling a power converter such that it presents a positive resistive load, also known as resistor emulation, has been shown to be a highly efficient method of scavenging maximum energy from a number of wireless power sources with a nearly constant equivalent output resistance ranging from RF to piezo-electric at very low power levels [2-5]. This method is advantageous at these very low power levels where traditional maximum peak-power tracking techniques cannot be used due to their higher power consumption or high input voltage requirement [6-8]. Prior resistor emulation solutions have enabled wireless sensors to function indefinitely at input power levels as low as 100 µW [9]. However, systems built from commercially available discrete parts are limited by their power consumption and size. Custom integrated circuits (ICs) have been developed for low input power and voltage levels and applied to energy scavenging [10-11], but they do not optimally load the input source for maximum scavenging efficiency over a wide range of operating conditions.

This paper presents an ultra low power energy scavenging IC that provides a programmable range of input resistances for optimal matching to energy sources and transfers the energy with high efficiency to a range of typical battery voltages. The emulated input resistance and converter parameters can be fixed for the lowest power operation or programmed digitally with an external microcontroller for system optimization at higher power levels. The IC is powered directly from the output battery voltage and can be used for extending battery life in low power wireless systems. The design operates efficiently with input voltages below 100 mV and with output battery voltages as low as 1.4 V, but requires a battery voltage of at least 1.95 V at startup. An overview of the energy scavenging IC is presented in Section II, including design details on key circuit components. Experimental results of the IC in a boost converter topology with an RF rectifying antenna (rectenna) as the wireless power source are provided in Section III demonstrating significantly improved energy scavenging efficiency from [2] with input power ranging from 265 µW down to less than 1 µW.

II. IC DESIGN OVERVIEW

As presented in [2-3], a boost converter can be controlled using two simple oscillators such that it operates in pulsed fixed-frequency discontinuous conduction mode (DCM). The resulting positive emulated resistance at the input port is given by [2]

$$R_{em} = \frac{V_{in}^2}{P_{in}} = \frac{2 \cdot L \cdot T_{hf}}{t_1^2 \cdot k}\left(\frac{M-1}{M}\right), \text{ where } M = \frac{V_{out}}{V_{in}}. \quad (1)$$

The parameters that determine the emulated resistance are the converter filter inductance, L, the transistor on-time, t_1, the high-frequency period, T_{hf}, and the low-frequency converter operation duty cycle, k. These parameters are shown in Fig. 1(a) as they relate to the inductor current, i_L, and the gate-drive voltage v_{gate}. As the boost converter is designed for very low input power, it is assumed that $V_{in} << V_{out}$ and thus the input voltage dependent term in (1), $(M-1)/M$, is essentially unity.

This converter control approach is transferred to an IC implementation. A block diagram showing the general organization of the energy scavenger IC is shown in Fig. 1(b). The on-chip power MOSFET can be the low-side switch in a boost, flyback, or floating input buck-boost converter depending on how the DRAIN pin is connected to the rest of the power stage. In this paper, a boost converter power stage is used as it is more efficient in low power and low input voltage conditons. A diode rectifier is used in the power stage instead of an additional on-chip power MOSFET for synchronous rectification as the control circuitry associated with switching the synchronous MOSFET would typically be more than the losses in the diode at low input power levels.

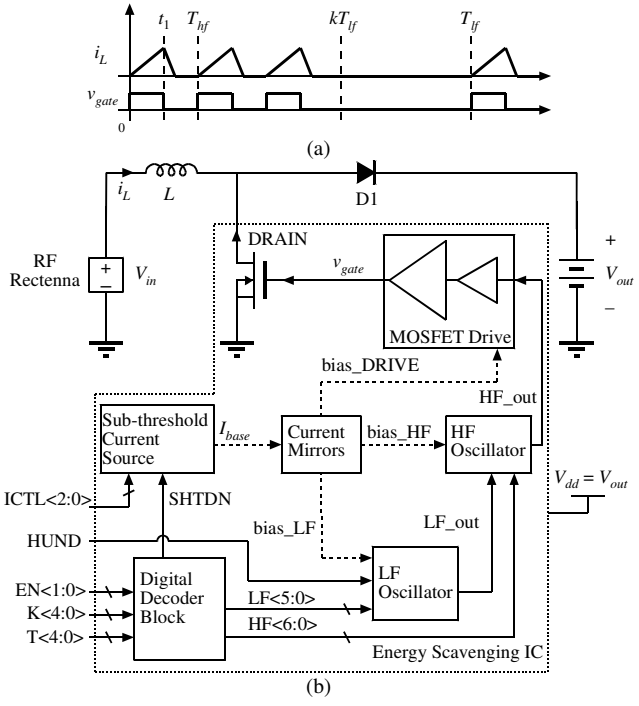

Fig. 1: (a) Ideal inductor current and gate-drive voltage waveform. (b) Block diagram showing the main components of the energy harvesting IC in a boost converter.

A. *Sub-threshold Current Source*

The sub-threshold current source provides an

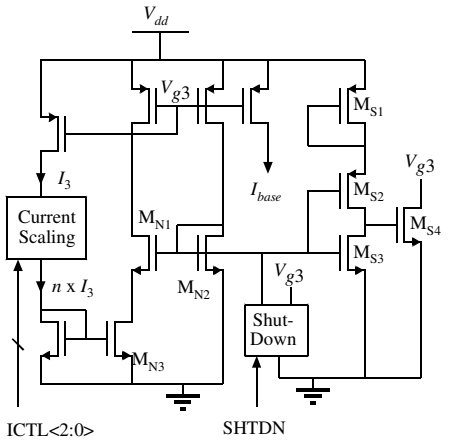

Fig. 2: Schematic of sub-threshold current source. The current scaling block adjusts the bias to MN3 that acts as a resistor. M_{N1} and M_{N2} operate in sub-threshold. When EN<1:0> = 00, SHTDN is set and the shutdown block disables the current sources. The devices M_{S1} – M_{S4} make up the boot-strap circuit that restarts the current source.

ultra-low base current (I_{base}) to the rest of the circuitry in the IC. This base current has a minimum value of 1.8 nA and is adjustable up to 10 nA via the digital control inputs ICTL<2:0>. The schematic of the sub-threshold current source is shown in Fig. 2. The design procedure is based on a resistorless ultra-low current reference [12]. The devices M_{N1} and M_{N2} are in sub-threshold operation and M_{N3} acts as a resistor set by the scalable current I_3. Most of the devices have long channels for low current operation. The sub-threshold devices, M_{N1} and M_{N2} have larger aspect ratios.

A digital input of EN<1:0> = 00 sets SHTDN and disables the current source, thus bringing the energy scavenger IC into shutdown mode in which it consumes less than 100 pA. When the IC is re-enabled, a boot-strap circuit (devices M_{S1} – M_{S4}) restarts the current source in less than 7 ms. Due to the ultra-low quiescent current requirement of the boot-strap circuit, a supply voltage of 1.95 V is required to start-up the current source. However, once the IC is enabled, it can operate down to supply voltages of 1.4 V. The minimum startup voltage was designed based on the application of extending battery life in wireless devices, where 2 V is a typical minimim voltage for reliable operation of lithium based rechargable batteries. The IC would have to be modified with an internal charge pump to startup with zero initial energy in the battery. The temperature coefficient of the current source is approximately 1248 ppm/^{o}C.

B. Low-frequency Oscillator

The LF oscillator block generates a low-frequency clock signal (LF_out) with an adjustable duty cycle, *k*, that pulses the HF oscillator output on and off. A simplified schematic of the LF oscillator is shown in Fig. 3(a). The oscillator operates based on the charge and discharge of a capacitor whose voltage varies within the hysterisis band of a schmitt trigger. The current I_{LF} is scaled from the base current generated by the sub-threshold current source in the current control block. The low-frequency duty cycle, *k*, is adjusted via digital inputs LF<5:0> that set the discharge current of the capacitor while the charge current remains fixed at 600 µs. Thus the frequency of the LF oscillator varies as *k* ranges from 0.03 to 0.9. The non-linearity of the discharge period is less than 0.25 % and from Monte Carlo

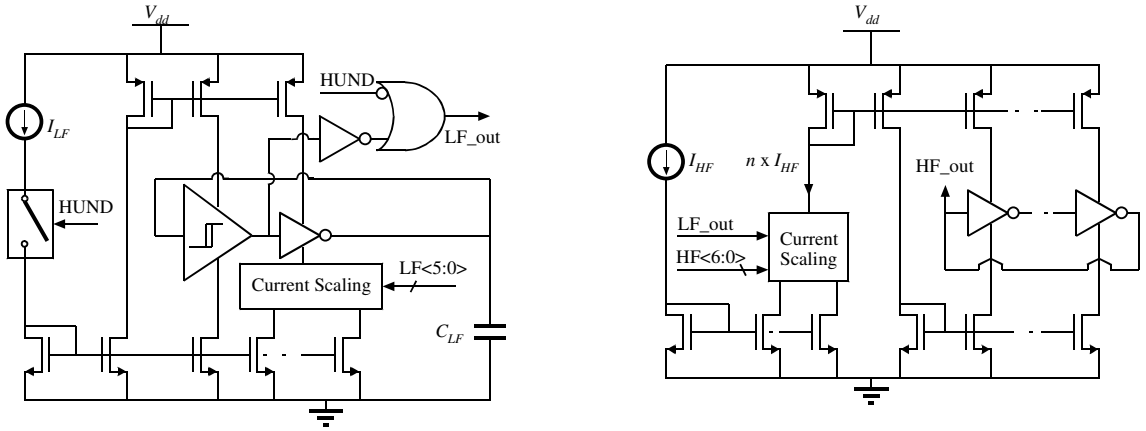

Fig. 3: (a) Simplified schematic of low-frequency oscillator circuitry. The current scaling block controls the current that discharges the timing capacitor, C_{LF}, and thus adjusts the k parameter. HUND removes power to the low-frequency oscillator and provides a constant on signal to the high-frequency oscillator. (b) Simplified schematic of high-frequency oscillator circuitry. The current scaling block controls the current supplied into the elements of the current-starved ring oscillator and thus the t_1 parameter.

simulations the standard deviation of a given k is, at worst, 2.3 %. An additional digital input bit, HUND, is used to for $k = 1$. This bit disables the LF oscillator and provides the HF oscillator with a constant on signal that keeps the output enabled at all times.

C. High-frequency Oscillator

The HF oscillator consists of three current-starved ring oscillators that generate a high-frequency signal (HF_out) with an on-time of t_1, where 2 x $t_1 = T_{hf}$. The t_1/T_{hf} ratio is selected as part of the ring oscillator design and to enusre DCM operation for a range of input power levels and emulated resistances. This signal is then passed to the on-chip power MOSFET gate-drive circuitry. With the 2 x $t_1 = T_{hf}$, the equation for the emulated resistance (1) simplifies to

$$R_{em} = \frac{V_{in}^2}{P_{in}} = \frac{4 \cdot L}{t_1 \cdot k}, \text{ where } V_{in} << V_{out}. \qquad (2)$$

The three ring oscillators are designed specifically for three battery voltages: 2.5 V, 3.3 V, and 4.15 V. Thus for each battery voltage, the range of t_1 will remain 0.5 µs < t_1 < 80 µs (12.5 kHz < f_{HF} < 1 MHz) for the corresponding ring oscillator. Each ring oscillator consists of 15 elements. The ring oscillator to be used is selected via EN<1:0>, and the other two are shutdown. Fig. 3(b) shows a simplified schematic of one of the current-starved ring oscillators and a current scaling block. The digital inputs HF<6:0> set the scaling factor n of the HF oscillator base current I_{HF}. This adjusts the current fed into the ring oscillator and thus the frequency of its output. Monte carlo simulations predict a standard deviation of no greater than 4 % for all frequencies. The non-linearity of the each oscillator is less than 1 %.

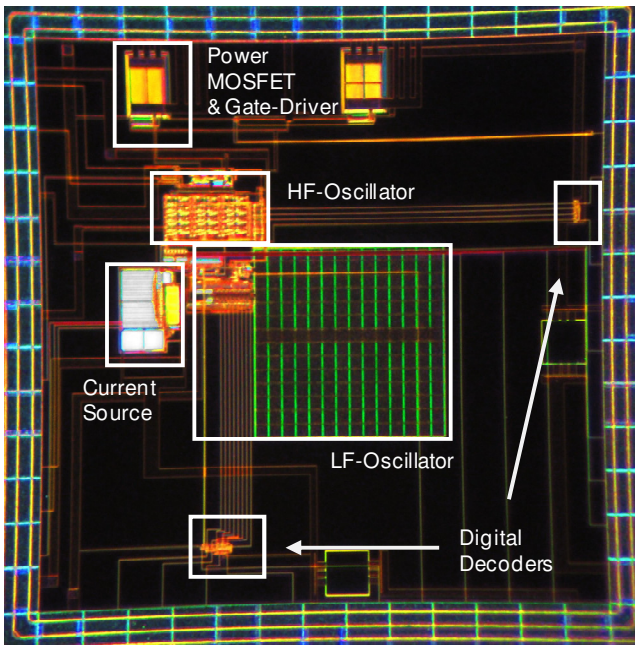

Fig. 4: Microscope image of energy scavenger IC fabricated in 5 V, 0.35 µm CMOS process. The various circuit components are labeled. The dimensions of the chip are: 2 mm x 2 mm.

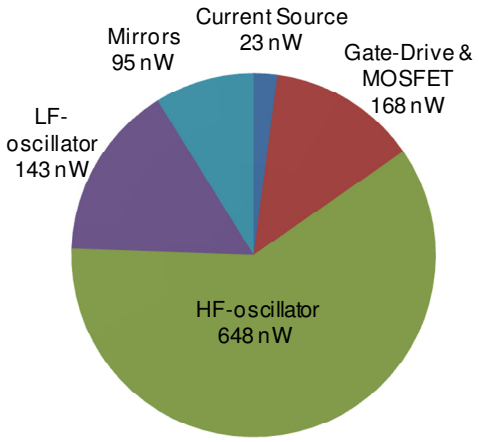

Fig. 5: Simulated power consumption of different components in the IC for $k = 0.26$ and $t_1 = 10$ µs.

including thin film lithium battries that have a nominal consumption of each circuit component is shown in Fig. 5. considered negligible.

The output of the LF oscillator, LF_out, controls whether the ring oscillator is on or off. When LF_out is low, no current ($n = 0$) is supplied into the ring oscillator and the output, HF_out is pulled low.

D. Additional Circuit Components

The additional features in the energy scavenger IC include a non-overlapping MOSFET gate-drive chain that eliminates IC power consumption from shoot-through currents. The on-chip power MOSFET sizing and gate-drive chain tapering is designed for optimal efficiency of a converter operating at sub-100 µW input power levels. The optimization is done with a modified process similar to that shown in [13]. The on-chip power MOSFET has an on resistance of $R_{ds\_on} = 2.1\ \Omega$ and an estimated gate capacitance of $C_{gs} = 1.19$ pF. The energy harvester IC was fabricated in a 5 V, 0.35 µm CMOS process. Fig. 4 shows a microscope image of the IC die and the various circuit components are labled. A 5 V process is used so that the IC can operate at most common battery voltages, voltage of $V_{batt} = 4.15$ V [14]. The predicted power The power consumption of the digital decoder block is

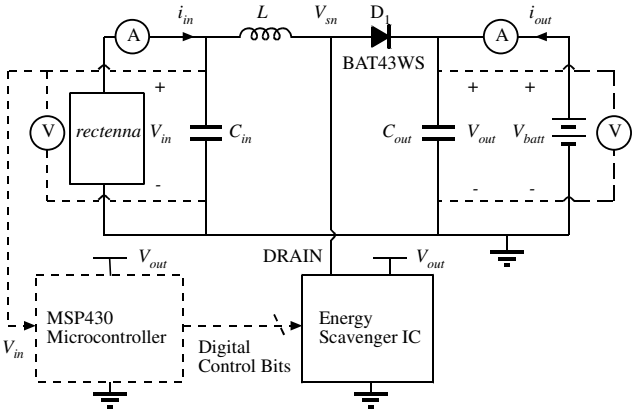

Fig. 6: Schematic of experimental test setup for energy scavenger IC used in a boost converter topology with an RF rectenna as the input power supply. The use of the IC along with an ultra-low power microcontroller is also investigated.

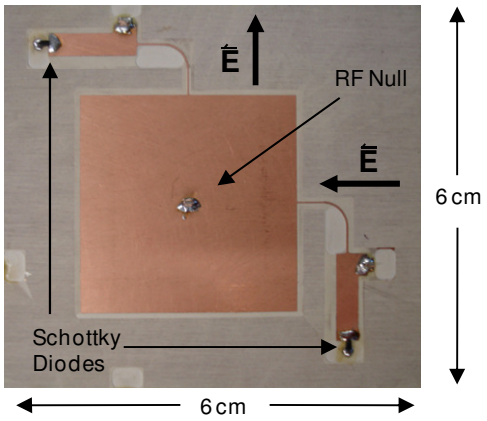

Fig. 7: RF rectifying antenna used. The design is similar to the rectenna presented in detail in [2] except with an optimal resistance of 500 Ω.

III. EXPERIMENTAL RESULTS

The fabricated energy scavenger IC is tested in a boost converter topology using the experimental setup shown in Fig. 6. The IC is powered directly from the converter output, V_{out}. The input and output capacitors, C_{in} and C_{out}, are 60 µF and 20 µF ceramic capacitors, respectively. The total output current, i_{out}, to a voltage source simulating a battery, V_{batt}, is measured using a calibrated Agilent 34411A multi-meter. This output current includes the current consumption of the energy scavenger IC along with the converter output current. Expermental timing parameters of the energy scavenger are discussed in Section III.A below. Section III.B presents experimental results of the IC used to harvest energy from an RF rectenna power source (Fig.7). Use of the energy scavenger IC together with a low power Texas Instruments MSP430 microcontroller for auto-tuning and configuration is discussed and experimental results are presented in Sect. III.C.

A. *Energy Scavenger IC Experimental Timing*

The range of the low-frequency oscillator duty-cycle is found to be from $k = 0.03$ to $k = 1$. The positive pulse period varies by 10 %, but the actual k parameter varies by less than 3 %. There is a higher resolution between k selections below $k = 0.3$ by design, as the energy scavenger IC is designed for relatively low input power levels where a low k parameter is required for achieving good boost converter efficiency. Varying the supply voltage while keeping LF<4:0> fixed does not affect the k control parameter significantly as the current ratios in the LF oscillator remain the same. The low-frequency period will change with V_{batt} as the hysteretic band of the current-starved Schmitt trigger will vary with the supply voltage.

The full range of transistor on times is 0.5 µs < t_1 < 80 µs for V_{batt} = 2.5 V. The experimentally found values for t_1 can vary by up to 10 % from their designed values depending on the part tested, but the non-linearity error remains under 1 %. For fixed digital inputs EN<1:0>, ICTL<2:0>, and HF<6:0>, t_1 will vary with V_{batt} due to the change in absolute currents and the propagation delay of an individual current-starved inverter in the ring-oscillator chain. The energy scavenger IC is tested from -5 °C to 55 °C and the timing parameter t_1 varies +5% and -6% respectively from the specified t_1 at room temperature. The low-frequency period is not affected by temperature, and thus the emulated resistance does not vary significantly with temperature.

For an example filter inductance, L = 330 µH, and D_1 = 0.5, the range of k and t_1 available results in a large range of achievable emulated resistances based on (2), ranging from 16.5 Ω < R_{em} < 88 kΩ.

B. Fixed Emulated Resistance Timing

The energy scavenger IC was tested in a boost converter power stage with the DRAIN pin connected to the converter switch-node, V_{sn}, of Fig. 6. The secondary switch is a Schottky diode (BAT43WS) with a nominal forward voltage drop of $V_D \approx 0.35$ V. The input power source is an RF rectenna shown in Fig. 7 and is similar to the patch rectenna discussed in detail [2], but with an optimal load resistance of 500 Ω. To select the value of the external filter inductance, L, and the timing parameters, k and t_1, the design procedure in [2] is modified for losses specifically associated with the energy scavenger IC. Total power losses of the boost converter and the IC are still defined as the sum total of conduction, switching, and control losses:

$$P_{loss} = P_{cond} + P_{sw} + P_{ctrl}\text{, where}$$
$$P_{ctrl} = P_{fix}\left(k, f_{lf}\right) + P_{pwm}\left(f_{hf}\right)\cdot\left(k + \frac{t_{settle}}{T_{lf}}\right) \quad (3)$$

The values of P_{fix} and P_{pwm} for the energy scavenger IC are determined during the experimental timing measurements of Section III.A. For V_{batt} = 2.5 V and low k, the power consumption of the LF oscillator, current source, and current mirrors combined is approximately P_{fix} = 275 nW and does not change significantly with V_{batt}. For a given supply voltage, the curve formed by the corresponding t_1 and supply current combinations is then used in efficiency optimization simulations as a control power loss that is a function of t_1, $P_{pwm}(t_1)$. Note that the HF oscillator in the IC has a settling time of approximately 40 µs, which is considered small enough to ignore (t_{settle} << T_{lf}). In addition to editing P_{fix} and P_{pwm} in converter efficiency optimization simulations, switching power losses associated with the

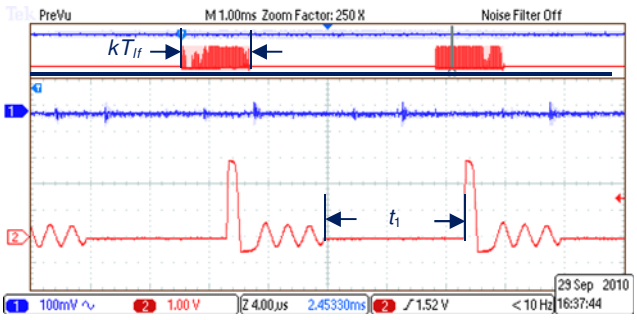

Fig. 8: Experimental waveforms of the boost converter input voltage (Ch1) that is AC-coupled and the switch-node voltage (Ch2). The pulsing action of the boost converter can be seen in the zoomed out view (top). The parameters are: t_1 = 10 µs and k = 0.26.

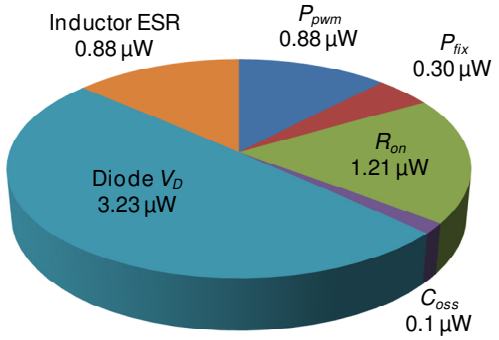

Fig. 9: Calculated power loss distribution at P_{in} = 30 µW. The parameters are: t_1 = 10 µs, k = 0.26, and L = 330 µH.

on-chip power MOSFET gate capacitance, C_{gs}, are removed from P_{sw} as these are now included in P_{pwm}.

With the modified boost converter power loss equations in place, efficiency optimization calculations similar to [2] are run for the desired emulated resistance, R_{em} = 500 Ω. These result in the selection of L = 330 µH as the discrete filter inductor in the boost converter power stage. This value provides the best maximum possible converter efficiency (variable t_1 and k) for a range of low input power levels (1 µW ≤ P_{in} ≤ 150 µW).

Next, the power loss calculations are run again at various input power levels with L = 330 µH to find timing parameters that maximize converter efficiency at a specific P_{in} whilst achieving R_{em} = 500 Ω. As the input power level increases, the t_1 that maximizes converter efficiency decreases as conduction losses in the power stage become more significant and control losses become a smaller percentage of the total power losses. The low-frequency duty-cycle, k, increases appropriately with decreasing t_1 to maintain R_{em} = 500 Ω.

For P_{in} = 30 µW, the optimal timing parameter combination is t_1 = 10 µs, k = 0.26. Fig. 8 shows the experimental waveforms of the input-voltage (Ch. 1) and switch-node voltage (Ch. 2) at these parameter settings. The power loss distribution at this input power level and timing parameter combination is given in Fig. 9. The largest power loss component is from the diode rectifier forward voltage drop V_D. One possible improvement is use of a synchronous rectifier. However, with the diode loss at 3.23 µW, it is challenging to achieve lower loss with the fast current sensing and precise timing control required to maintain DCM operation with the short diode conduction interval.

With these fixed R_{em} and timing parameters that maximize converter efficiency at P_{in} = 30 µW, the incident power to the RF rectenna input source is swept and the resulting converter efficiencies are found. The experimental converter efficiency, η_{boost}, versus P_{in} is shown in Fig. 10, including all control and power stage losses, for four timing parameter

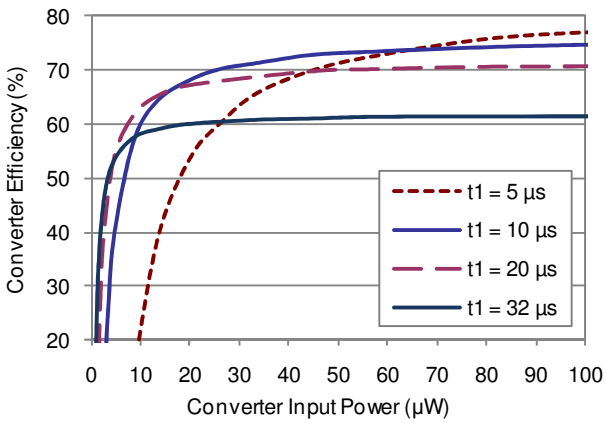

Fig. 10: Efficiency curves of the energy scavenger IC in a boost converter topology at four different control timing parameter combinations (t_1, k). Each combination optimizes converter efficiency for four different input power levels and for R_{em} = 500 Ω.

combinations: [t_1 = 32 µs, k = 0.08], [t_1 = 20 µs, k = 0.13], [t_1 = 10 µs, k = 0.26], and [t_1 = 5 µs, k = 0.48], that are optimized for P_{in} = 1 µW, 5 µW, 30 µW and 80 µW respectively.

Fig. 10 shows the maximum possible converter efficiency, with manual optimization of timing parameters as a function of input power P_{in}. That data is also presented in Table I with additional details. The experimental R_{em} shown in Table I remains within 5 % of the desired value for optimal matching to the power source and maximum energy scavenging over a wide range of power levels. The results demonstrate positive energy harvesting at input power levels below P_{in} = 1 µW.

C. Microcontroller Controlled Emulated Resistance Timing

A low power microcontroller can be used to dynamically control the converter timing parameters for system optimization over a wide range of input power levels. The Texas Instruments MSP430 microcontroller was used in the setup of Fig. 6 to demonstrate this capability.

The microcontroller provides the digital control bits to the energy scavenger IC and operates in a deep sleep mode for the majority of the time. A user-defined value determines how often the microcontroller ADC (10-bit SAR) wakes up and samples the converter input voltage. Once the conversion is complete, the ADC powers down automatically. The converted input voltage value is used in a look-up table as an estimate of input power to adjust the digital control bits sent to the energy scavenger IC. This optimization requires prior knowledge of the input rectenna source characteristics and efficiency curves such as those shown in Fig. 10.

Experimental results are shown in Fig. 11, where the microcontroller sampling period is set at 1 s to minimize the increase in control power consumption. At a sampling frequency of 1 Hz, the microcontroller has a supply current of 375 nA. The new values of P_{fix} with the energy scavenger IC and microcontroller combined is approximately P_{fix} = 1212.5 nW (V_{batt} = 2.5 V). The increase in P_{fix} is evident in the efficiency plot of the energy scavenger IC with

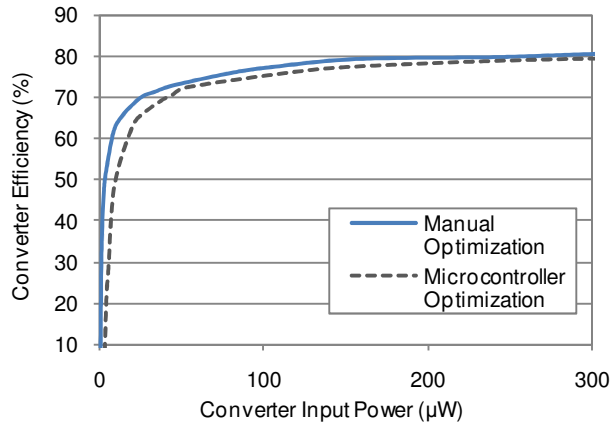

Fig. 11: Efficiency curves of the energy scavenger IC in a boost converter topology with manual and microcontroller optimization of control timing parameters, t_1 and k.

TABLE I
EXPERIMENTAL RESULTS WITH MANUAL ADJUSTMENT OF R_{EM} (V_{DD} = 2.5 V)

$P_{incident}$ (µW/cm^2)	η_{RF} (%)	P_{in} (µW)	V_{in} (mV)	R_{em} (Ω)	P_{out} (µW)	η_{boost} (%)
1.29	2.01	0.89	20.90	489	0.16	18.05
1.74	2.49	1.48	26.85	489	0.52	35.13
2.51	3.26	2.73	36.45	488	1.29	47.36
3.55	3.95	4.80	48.40	487	2.57	53.58
6.92	5.70	13.51	81.60	493	8.81	65.16
12.9	8.75	33.54	132.4	523	23.86	71.14
24.6	9.64	80.13	202.7	513	60.66	75.70
30.3	10.1	104.7	231.8	513	80.77	77.13
41.6	11.2	156.3	283.9	516	123.6	79.06
63.9	12.5	265.0	376.0	534	211.5	79.80

microcontroller optimization shown in Fig. 11. At very low P_{in}, the converter efficiency is greatly reduced. As P_{in} increases, the control power loss becomes a much smaller percentage of total power loss, and thus the increase in P_{fix} from the addition of the microcontroller has a negligible impact on converter efficiency. In typical wireless sensors, there is already a microcontroller present and the energy scavenging IC timing parameters could be controlled by the sensor load with a negligible increase in system power consumption or cost. Also, if the power source output resistance is known a-priori or varies in time, then the microcontroller can be used with the energy scavenger IC to occasionally perform a peak power tracking algorithm to search out the optimal emulated converter input resistance, as shown in [15].

IV. CONCLUSION

An energy scavenger IC that uses resistor emulation to optimally load an RF rectenna wireless power source has been shown to deliver positive output power at input power levels as low as 1 µW at converter efficiencies, η_{boost}, over 35 %. The IC uses simple, current-starved analog circuitry to control boost, buck-boost or flyback converters in fixed-frequency DCM operation and thus achieve a desired emulated resistance within the range 16.5 Ω ≤ R_{em} ≤ 88 kΩ for an external inductance of L = 330 µH. Experimental results demonstrate the energy scavenger IC in a boost converter topology maintaining an emulated resistance within 10 % of a designed value with fixed converter control timing parameters, t_1 and k, over a decade of input power levels, P_{in}. To maximize energy scavenging over a wider range of P_{in}, the converter control timing parameters are tuned using a Texas Instruments MSP430 microcontroller together with the energy scavenger IC. The design can operate efficiently with input voltages below 100 mV and with

output battery voltages as low as 1.4 V, but requires a battery voltage of 1.95 V at startup. Energy scavenging with the IC can be used for extending battery life in low power wireless systems. The experimental results presented are based on collecting RF energy, although the approach can also be applied to other energy sources that have an optimal load resistance, including energy transducers using wind, vibration, and temperature gradients.

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