High-Efficiency Harmonically-Terminated Rectifier for Wireless Powering Applications

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***Abstract*—In wireless powering, the rectifier efficiency has a large effect on overall system efficiency. This paper presents an approach to high-efficiency microwave rectifier design based on reduced conduction angle power amplifier theory. The analysis for an ideal rectifying device is derived to predict efficiency dependence on optimal dc load. A class-C 2.45 GHz Schottky-diode rectifier with short-circuit 2nd and 3rd harmonic terminations is designed using source-pull measurements, and demonstrates a maximum RF-DC conversion efficiency of 72.8% when matched to 50 Ω. The approach is applied to integration of a rectifier with a dual-polarization patch antenna in a non 50 Ω environment and free-space measurements demonstrate a lower bound on efficiency of 56% at 150 μW\cm^2 power density which includes matching circuit and mismatch losses.**

I. Introduction

The front-end receiving portion of a wireless powering system is an antenna feeding a rectifier, usually referred to as a rectenna. The RF-DC rectification efficiency of the rectifier determines the overall wireless power delivery efficiency, for both high-power directive wireless beaming, e.g. [1], and low-power harvesting, e.g. [2]. Other applications where rectifier efficiency is important are microwave power recycling [3], and DC/DC converters with extremely high frequency switching [4]. In many of the reported microwave rectifiers, filtering of the harmonics at both the input and output has been investigated, e.g [5], [6], mainly to reduce re-radiated harmonic power. However, the impact of harmonic terminations on the wave shaping and resulting RF-DC conversion efficiency has not been researched to the best of our knowledge.

Harmonic terminations are commonly applied to increase efficiency in power amplifiers (PA). The transistor nonlinearities generate harmonic content at the output, and in a number of high-efficiency amplifier classes, specific harmonic terminations are used to shape the current and voltage waveforms. In reduced conduction angle PAs (classes A, AB, B and C), all harmonics are shorted at the virtual drain reference plane in the transistor. In a rectifier, the nonlinear rectifying element also generates currents and voltages at the harmonics of the input frequency, and although in this case the output is at DC, the efficiency of the rectifier can also be modified by terminating the harmonics. Class-C will in this case have the highest RF-DC efficiency, as will be shown in the next section on the example of a single-diode rectifier. When all harmonics are presented with short circuits, a relationship between the optimal DC load and input impedance at the fundamental frequency can be derived. Experimental data at 2.45 GHz with a single-diode rectifier matched to 50 Ω validates the theory with a demonstrated rectification efficiency of 72.8% after the loss of the matching network is de-embedded, and compares well with harmonic balance simulations. Without explicit harmonic terminations enforced, the rectifier is 66% efficient. The harmonic termination concept for improving rectifier efficiency is integrated with a dual-polarized patch antenna for a wireless powering application.

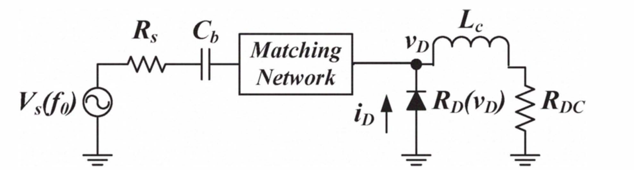

Fig. 1. Microwave rectifier circuit diagram. An ideal blocking capacitor C_b provides dc isolation between the microwave source and rectifying element. An ideal choke inductor L_c isolates the dc load R_{DC} from RF power.

II. Rectifier Analysis

Consider the microwave rectifier shown in Fig. 1. A sinusoidal microwave power source with voltage magnitude V_s and impedance R_s drives the rectifying element having a resistance denoted by $R_D(v_D)$ and defined as

$$R_D(v_D) = \begin{cases} \infty, & v_D > 0 \\ 0, & v_D \leq 0 \end{cases} \tag{1}$$

where v_D and i_D are the instantaneous voltage across and current through the rectifying element, respectively. The dc load seen by the rectifying element is R_{DC} while the load at the fundamental frequency f_0 and successive harmonics is set by the matching network. Assume the matching circuit presents $R_s(f_0)$ to the rectifying element with all subsequent harmonics terminated in short circuits. This is equivalent to the harmonic terminations for a canonical reduced conduction angle power amplifier. The motivation for analyzing short-circuit harmonic terminations rather than opens is the intention to build the rectifier with a Schottky diode which has a significant non-linear junction capacitance. Short-circuiting the harmonics fixes the harmonic terminations at the intrinsic diode by shorting out the non-linear junction capacitance.

When the incident RF voltage at the ideal rectifier swings negative, it is clipped at zero given (1). However, the enforced harmonic terminations force the voltage waveform to contain only a dc and fundamental frequency component. Therefore, a dc component must be produced by the rectifying element such that the voltage waveform maintains its sinusoidal nature. The

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voltage across the rectifying element can now be expressed as

$$v_D(\theta) = V_{DC} + V_D(f_0)\sin(\theta) \tag{2}$$

where $V_D(f_0)$ is the fundamental frequency component of the voltage across the rectifying element, V_{DC} is the dc component, $V_{DC} = V_D(f_0)$ and $\theta = 2\pi f_0 t$. The current waveform contains infinite frequency components, and is expressed as

$$i_D(\theta) = 2\pi I_{DC}\delta\left(\theta - \frac{3\pi}{2} - 2n\pi\right), \quad n = 0, 1, ..., \infty \tag{3}$$

where I_{DC} is the dc current and $\delta(\theta)$ is the Dirac delta function.

When all available input power is delivered to the rectifier, the RF-DC conversion efficiency is 100% because the rectifying element is ideal and cannot dissipate power itself. In order for all available input power to be delivered to the rectifier, it is straightforward to show that the dc load must be set relative to the fundamental frequency load as

$$R_{DC} = 2R_s(f_0) \tag{4}$$

A harmonic balance simulation of an approximately ideal rectifier with short-circuited harmonic terminations was performed in Microwave Office using the SPICE diode model with no parasitics (PNIV) as the rectifying element. The device temperature was set to 1° K to approximate an ideal switch. The fundamental frequency excitation was set to 1 W at 1 GHz with the first 200 harmonics being terminated in short-circuits. The diode was presented with 50 Ω at the fundamental frequency and the dc load was swept from 5 Ω to 200 Ω. The simulated data is then normalized to generalize the simulation results. The ideal time-domain current and voltage waveforms across the diode are shown in Fig. 2 with the RF-DC conversion efficiency as a function of $R_{DC}/R_s(f_0)$ for varying rectifier on-resistance being shown in Fig. 3. It is clear that the mechanism of operation in the ideal case agrees with the theory presented above. The reduction in RF-DC conversion efficiency when the DC load is not set according to (4) is simply due to a fraction of the incident power being reflected due to the impedance mismatch.

The waveforms in Fig. 2 are identical to those of a class-C PA as the conduction angle approaches 0°. The parasitics of realistic rectifying devices such as on-resistance, non-linear capacitance and threshold voltage will cause actual implementations of the harmonically terminated rectifier to deviate significantly from theory, but it is instructional to understand the mechanism of efficient rectification nonetheless.

III. Rectifier Circuit

The Skyworks SMS7630 Schottky diode in the SC-79 package was selected for the half-wave rectifier [7]. Source-pull was performed at 2.45 GHz with 0-10 dBm available input power for various dc loads in order to identify the combination of input power, fundamental load and dc load resulting in highest efficiency. The best case occurred at 6 dBm input power, with the source-pull contours being shown in Fig. 4. The on-resistance of the SMS7630 is 20 Ω with the optimal DC load being found as 1080 Ω, therefore R_{ON} is approximately 2% of R_{DC} which in theory is 4% of $R_s(f_0)$. From Fig. 3, a peak efficiency of 87% occurs with infinite harmonic terminations, therefore the achieved 77.6% is very reasonable considering only the 2nd and 3rd harmonics were explicitly terminated.

Measurements of a rectifier designed using the source-pull data show a maximum RF-DC conversion efficiency of 72.8%

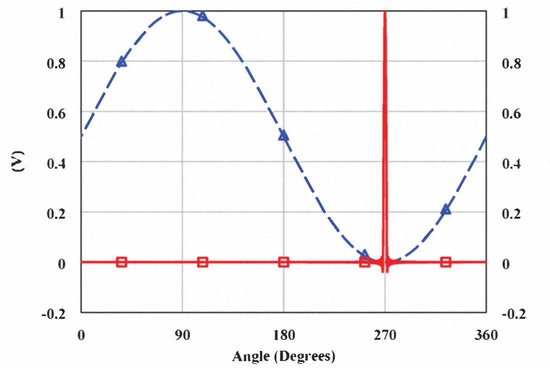

Fig. 2. Ideal normalized voltage (dashed) and current (solid) waveforms for reduced conduction angle half-wave rectifier. The waveforms have been normalized to their peak values.

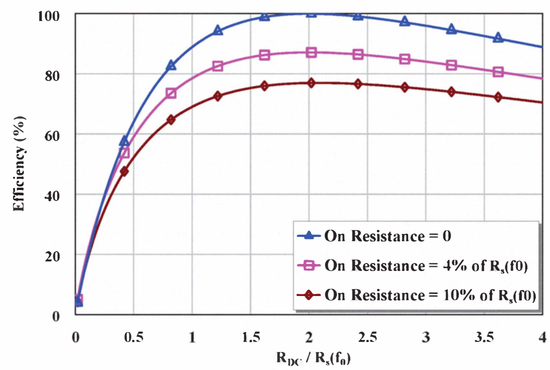

Fig. 3. Simulated efficiency of reduced conduction angle half-wave rectifier versus $R_{DC}/R_s(f_0)$ for varying rectifier on-resistance.

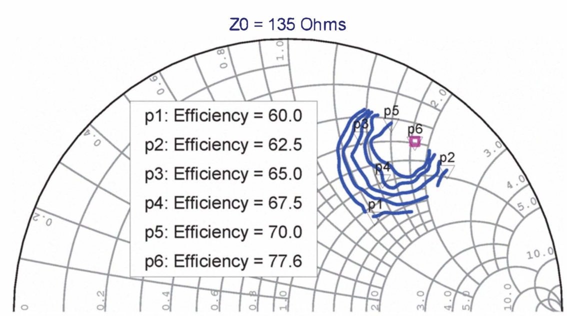

Fig. 4. Source-pull contours with available input power to the diode set to 6 dBm. The impedance is referenced to the junction capacitance of the diode, therefore the lead inductance of the package has been compensated for. Setting R_{DC} to 1080 Ω was found to result in the optimal efficiency for this input power.

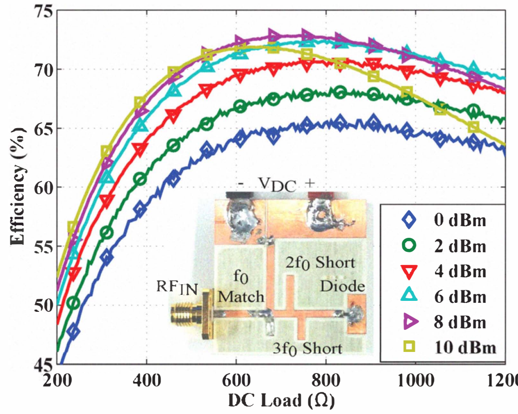

Fig. 5. RF-DC conversion efficiency versus dc load fixed available input powers with 0.6 dB matching network loss de-embedded. The maximum efficiency of 72.8% occurred at 8 dBm with R_{DC} = 742 Ω, which is lower than the 1080 Ω found during source-pull. However, the efficiency at 1080 Ω is 69.9% which is very close to the peak value.

when matched to 50Ω being obtained after the 0.6 dB matching network loss is de-embedded. The fabricated rectifier and dc load sweep measurements are shown in Fig. 5. Open circuit shunt stubs were used to present short-circuit terminations at the second and third harmonic. A shunt capacitor was used for presenting the fundamental frequency impedance to reduce size and allow tunability. The reduction in efficiency relative to the source-pull measurements is due to the matching circuit not presenting the ideal impedance found during source-pull.

IV. Improving Wireless Powering Efficiency

The class-C rectifier can be applied to improving the efficiency of a wireless powering reception device. We demonstrate the concept on the example of a dual-linearly polarized patch rectenna, with a rectifier circuit for each polarization (Fig. 6). In this circuit, the first 5 harmonics are shorted and the impedances are validated by calibrated measurements. Fig. 6 shows the simulated vs. experimentally achieved harmonic terminations. Fig. 7 shows the simulated time domain waveforms corresponding to these terminations, with higher harmonics not explicitly terminated in the harmonic balance simulation, as compared to the infinite number of shorted harmonics shown in Fig. 2. The rectenna is fabricated and measured in a free-space calibrated measurement system, by measuring the incident power density on the rectenna and multiplying by the physical antenna area (64 cm^2) to determine incident power on the rectifier. The efficiency calculated from the measured dc output in this case is 56% at 150 $\mu\mathrm{W/cm}^2$ power density (9.6 mW total power), which includes antenna and matching circuit losses and is a lower bound on efficiency, and is slightly lower than measured for the rectifier in Fig. 5.

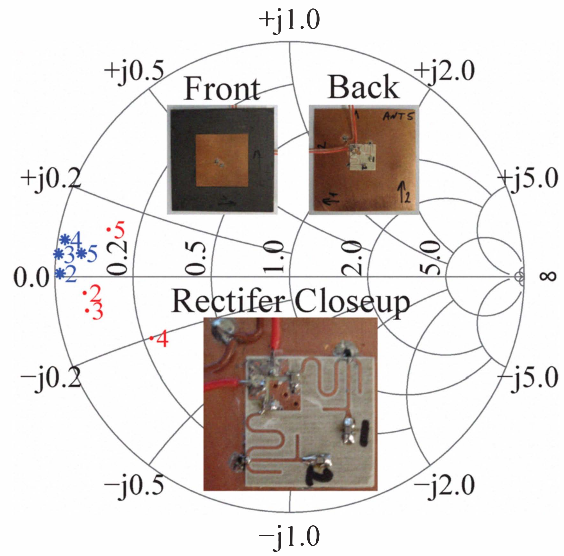

Fig. 6. Dual-linearly polarized patch rectenna and associated $2f_0$-$5f_0$ terminations (50 Ω Smith Chart). Blue and red indicate the simulated and measured harmonic terminations, respectively. The rectifiers are dc isolated.

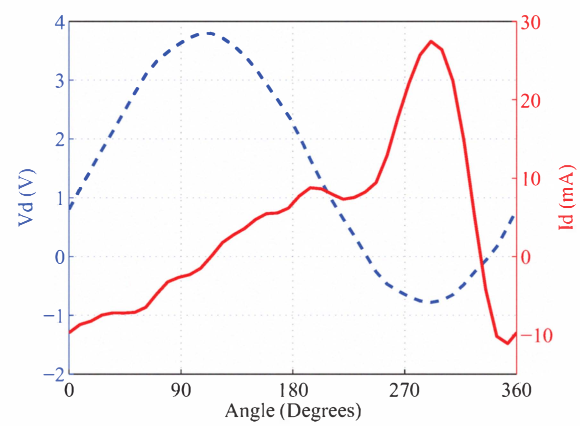

Fig. 7. Simulated time-domain current and voltage waveforms for rectifier used in dual-polarized patch antenna (using SMS7630 diode). The frequency and input power were set to 2.45 GHz and 10 dBm, respectively.

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