A MMIC/Hybrid High-Efficiency X-Band Power Amplifier

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***Abstract*— This paper presents design and measurements of a X-band high-efficiency MMIC/hybrid PA implemented in the TriQuint 0.25-um GaN on SiC pHEMT process. In the absence of a nonlinear model valid for high-efficiency classes of operation, an output network with specific harmonic terminations is included in the MMIC, allowing for external fundamental load-pull only. The results show a power added efficiency (PAE) of 71% with a saturated gain of 12 dB and output power of 3 W, or 4.5 W/mm, at 9.8 GHz in CW operation.**

***Index Terms*— Power Amplifier, MMIC, Hybrid, Load-Pull.**

I. Introduction

Power amplifiers with power levels above 1 W at frequencies around 10 GHz have achieved efficiencies as high as 67% as summarized in Table I, where most of the recent PAs are fabricated monolithically with GaN transistors. When designing for high efficiency, a good nonlinear device model is essential, and in its absence, usually the designer resorts to load/source pull measurements [1]. Since high efficiency PAs usually rely on specific terminations at harmonic frequencies at the output, the load-pull setup should have not only fundamental-frequency tuners, but also second and third harmonic tuners, which are expensive and not readily available at high frequencies. In [2], [3] methods for load-pull measurements with fixed class-E and class-F^{-1} are presented, respectively. The device test circuit contains specific harmonic terminations that are present during the load-pull measurements at the fundamental.

In this paper, we extend the fundamental-only load pull design method for harmonically-terminated PAs to a semi-hybrid 10 GHz 3 W power amplifier designed in the 0.25 μm TriQuint Semiconductor 3MI GaN process. The device, pre-matching circuit, biasing circuit and harmonic terminations are implemented in a MMIC, while the final fundamental frequency matching is designed off-chip. The paper presents the MMIC design and hybrid load-pull data.

II. MMIC Design

To obtain over 3 W of output power at 10 GHz, a 10-finger pHEMT with 70 μm gate width is chosen, since the 0.25 μm GaN process yields 5-7 W/mm of output power [8]. The output capacitance of the device is extracted from measured S-parameters using the method presented in [9] and found to be:

TABLE I

Ref	$f\,(GHz)$	$P_{out}\,(W)$	$PAE\,(\%)$	$Comment$
[4] 1999	3-9	3.2	24	GaN, > octave BW distributed
[5] 2009	1.5-17	9-15	20-38	GaN, > decade BW
[2] 2005	8	0.3	52	InP, class-E
[6] 1999	8.4	1.7	57	Hybrid GaAs class-E
[7] 2007	7.5	4.79	67	GaN, class-E pulsed
This Work	9.8	3.26	71	MMIC/hybrid, GaN load-pull, class-F^{-1}

$$C_{out} = C_{ds} + C_{gd}||C_{gs} = 0.248\,\mathrm{pF} \tag{1}$$

or about 0.354 pF per mm of gate periphery.

The small output capacitance lends itself to a class-F^{-1} design in which the voltage across the drain is peaked, utilizing the high breakdown voltage of GaN. The second and third harmonics are open and short-circuited at the virtual drain, respectively, and are implemented using shunt capacitors for resonators, as shown in Fig. 1, circuit N. The fundamental impedance at the virtual drain is pre-matched to approximately 70 Ω. At 10 GHz 0.63 dB insertion loss of the output pre-matching circuit is achieved. Simulations show that the terminations at the second and third harmonics are relatively fixed, while the fundamental impedance may be tuned substantially, within a $\mathrm{VSWR} = 9$ circle.

For design simplicity, the gate bias tee is matched to 50 Ω on both RF ports such that once the matching circuit is designed the bias tee can simply be added to the circuit without transforming the match. The gate bias tee design is simpler due to low DC handling requirements which allow a spiral inductor to be used as an RF choke. A 10 Ω low frequency stabilization resistor limits the current handling to 54 mA. The design exhibits return loss better than 24 dB, isolation better than 25 dB, and insertion loss less than 0.10 dB over the entire 8-12 GHz band.

In the drain bias circuit, due to the high DC current handling requirements, a meandered transmission line is designed to effectively act as the RF choke. A coupled line model is used to arrive at a design resulting in 90° of phase at the design frequency of 10 GHz. The line is shorted to ground through a 10 GHz shunt resonant capacitor, making it an RF open to the through line. The design shows an

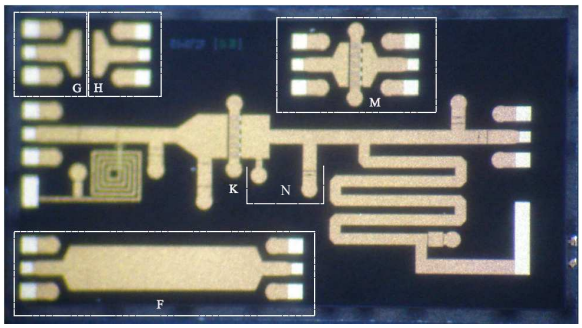

Fig. 1. Photo of the fabricated 2 mm x 4 mm MMIC. The main amplifier is circuit (K) with the test and calibration circuits (F-H,M). Note the on-chip second and third harmonic terminations (N).

insertion loss of 0.18 dB and an RF-DC isolation of 30 dB at 10 GHz.

Prior to designing the load pull input matching circuit, the nominal impedance to present to the device must be defined. This is done by simulating the fundamental frequency input impedance of TriQuint's non-linear model while varying the fundamental frequency load presented to the drain in small-signal. The conjugate of the simulated impedance gives a good approximation of the impedance to present to the gate of the transistor. Of course the source tuner will be used to modify this impedance, but it is preferable to pre-match to a good location to maximize the validity of the calibration. Based upon the results, a 5 Ω pre-match impedance at the fundamental frequency is selected. The circuit uses a linear taper and two shunt capacitors to provide an inductive match with near 5 Ω real part as shown in Fig. 1, circuit K. The insertion loss of the match at 10 GHz is 0.62 dB which is large but expected due to the dramatic impedance transformation (10:1).

III. Load Pull Measurements

The scattering parameters of the input and output pre-matching circuits are measured using on-wafer TRL calibration kits for load pull calibration and impedance verification. A slight frequency shift occurred moving the input pre-matched impedance from $5 + j1.5\Omega$ to $7.4 + j5.9\Omega$ which is still sufficient for source pull. The measured insertion loss of the fixture at 10 GHz was 0.60 dB, only 0.03 dB lower than simulated. Since the insertion loss and pre-matched impedance agree with simulations, the RF-DC isolation is assumed to be satisfactory.

Fig. 2 compares the simulated and measured output pre-matching fixture impedance match. After measuring the output pre-matching circuit, the best performance is observed at 9.79 GHz. Table II lists the measured fundamental, second harmonic, and third harmonic terminations for the output fixture at both 10 GHz and 9.79 GHz. The 20 GHz impedance is low and complex, while the 19.6 GHz impedance is high (300Ω) and nearly purely

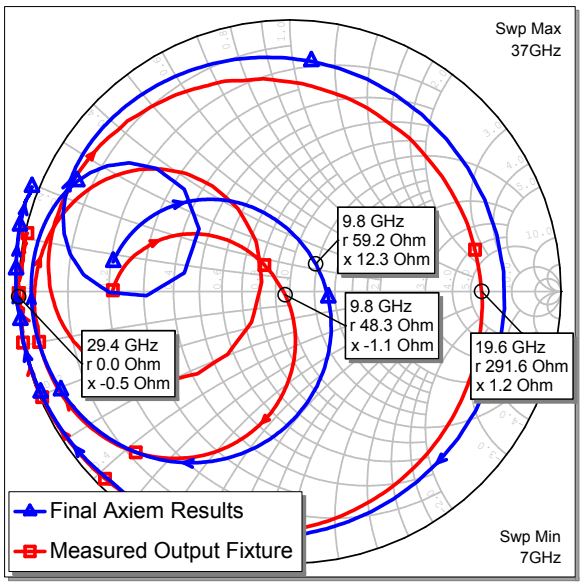

Fig. 2. Simulated versus measured output pre-matching fixture impedance match. The measured results are slightly shifted in frequency relative to the simulation. The Smith Chart is normalized to 50 Ω.

TABLE II
Output Impedance Deembedded at the Virtual Drain

f_0 = 10 GHz	f_0 = 9.79 GHz
$Z(f_0)$ = 50.2 - j11.8 Ω	$Z(f_0)$ = 48.3 - j1.1 Ω
$Z(2f_0)$ = 25.9 - j90.6 Ω	$Z(2f_0)$ = 291.8 - j1.0 Ω
$Z(3f_0)$ = 0.0 + j0.9 Ω	$Z(3f_0)$ = 0.0 - j0.5 Ω

real. Therefore, the source and load pulls are performed at 9.79 GHz with class-F^{-1} terminations. Source pull is performed at the fundamental frequency for small signal gain at a quiescent point of 30 V and 40 mA with the load impedance set to 50 Ω. The peak small signal gain of 15.1 dB occurred at $3.1 + j16.3\Omega$.

Initial on-wafer load pull measurements are insufficient since the PAE contours could not be closed due to an insufficiently high fundamental pre-matched impedance. In addition, the tuning range is limited to $|\Gamma| = 0.5$ due to the loss of the matching circuit and probe-tuner cascade. The measured insertion loss of the fixture is 0.47 dB, which is lower than simulations using the PDK. A peak measured PAE of 51% is significantly lower than expected, with an output power of 34.5 dBm (2.8 W) [10].

In order to increase the range of the load pull measurements, additional pre-matching at the fundamental frequency is implemented in a MMIC/hybrid PA shown in Fig. 3. The input match and output fundamental pre-match circuits are fabricated on 30 mil Rogers 4350B substrate ($\varepsilon_r = 3.6$) and wire-bonded to the MMIC. The fundamental output pre-matched impedance was increased to $121 - j25\Omega$.

The load pull measurement is completed on the hybrid amplifier using a Focus Microwave single frequency tuner.

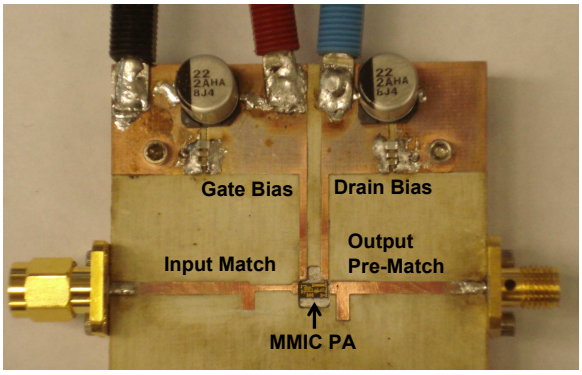

Fig. 3. Photograph of the MMIC/hybrid load pull circuit showing external matching at the fundamental.

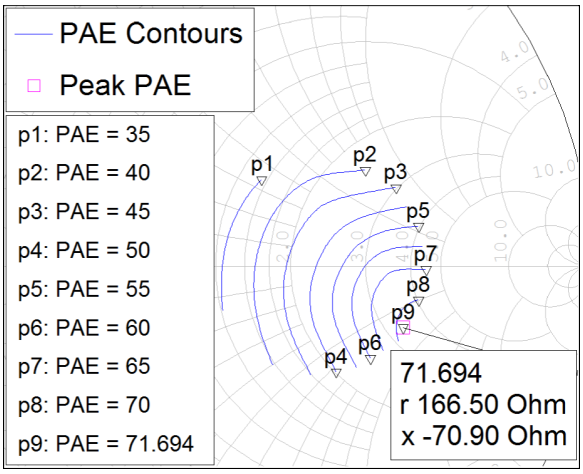

Fig. 4. Measured power added efficiency contours with 30V drain voltage and 40 mA quiescent current. The Smith Chart is normalized to 50Ω.

The measured MMIC fixtures, microstrip fixtures, and tuner S-parameters, along with the HFSS modeled bond-wire transition and extracted output capacitance are used to deembed the measurements to the virtual drain of the transistor. A peak power added efficiency was measured to be 71% as seen in Fig. 4 with an output power of 35.125 dBm (3.26 W) and a gain of 12 dB. A peak output power was measured to be 35.59 dBm (3.62 W), as seen in Fig. 5, at a PAE of 62 %.

IV. Conclusion

We show that a fundamental tuner that covers only a $|\Gamma| \leq 0.3$ circle can be effectively used for PA load-pull when the second and third harmonics are terminated on-chip, and the pre-matching circuit is implemented partly in a hybrid circuit. The load pull results show a power density of 4.5 W/mm, a PAE of 71%, and a drain efficiency of 75.75% in CW operation at peak efficiency at 9.8 GHz, which compares very well to the state-of-the-art results in [7] of 5.75 W/mm in pulsed mode at 7.5 GHz. This design

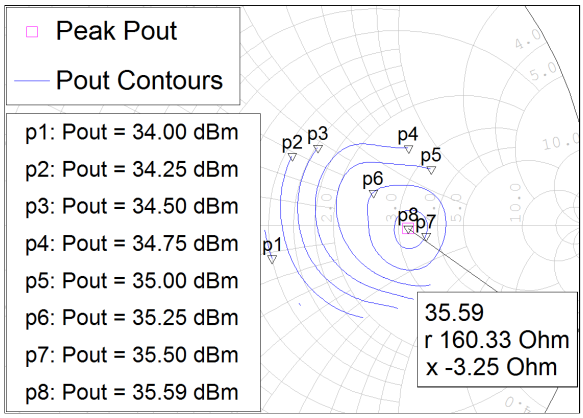

Fig. 5. Measured output power contours with 30V drain voltage and 40 mA quiescent current. The Smith Chart is normalized to 50Ω.

method is useful for any device when a nonlinear model is not available.

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