# X-Band MMIC GaN Power Amplifiers Designed for High-Efficiency Supply-Modulated Transmitters

Scott Schafer[1], Michael Litchfield[1], Andrew Zai[1], Zoya Popovíc[1], Chuck Campbell[2]

[1]Electrical Computer and Energy Engineering, University of Colorado at Boulder, Boulder, Colorado 80309
[2]TriQuint Semiconductor, 500 West Renner Rd. Richardson, Texas

***Abstract*—The design and measured performance of X-band power amplifier MMICs that utilize 0.15 $\mu$m GaN on SiC process technology are presented. Under continuous wave operating conditions these single and 2-stage MMICs demonstrate peak power added efficiencies (PAE) from 45% to 69%, output powers from 2.5-13 W, and up to 20 dB of large signal gain. Designed for drain modulated applications, the power amplifiers maintain good performance at reduced drain bias voltage. The output power of the two stage MMIC can be varied from 2 W to 13 W when the drain bias is varied between 7.5 V and 20 V while maintaining a PAE above 54%.**

***Index Terms*—MMICs, power amplifiers, Gallium Nitride**

## I. Introduction

Modern radar and communication signals have increasingly high peak to average ratios and bandwidths. It is desired that transmitters maintain high efficiency over these difficult operating conditions. Several architectures have been demonstrated to achieve high efficiency over envelope amplitudes: Doherty [1], [2]; outphasing (LINC) [3]–[5]; and various forms of envelope tracking overviewed in [6]. Many radar and communication systems operate at X-band, and recently a number of high efficiency amplifiers have been demonstrated in GaAs, InP, [7] and GaN with 5 W and PAE of 43-57% in pulsed mode [8] and 3.7 W with PAE of 61% in CW mode [9]. Various power amplifier topologies have been used to achieve high efficiency operation, most commonly class-E, F, $F^{-1}$, and J [1], [7], [9]–[12].

In this paper we present GaN MMIC power amplifiers (PAs) with power levels ranging from 2.5-13 W and PAE greater than 60%, specifically designed for high efficiency operation under drain supply modulation. To this end the circuits are designed to maintain acceptable levels of gain, power and efficiency at reduced power supply voltage.

## II. MMIC Design

### A. Process Technology and Model

The MMICs were fabricated in a 0.15 $\mu$m gate length process with an AlGaN/GaN epitaxial layer on 100 $\mu$m SiC on 100 mm diameter wafers. Typical DC characteristics of these transistors are $I_{max}$=1.15 A/mm, $g_{m,max}$=380 mS/mm, and 3.5 V pinch-off at $V_{ds}$=10 V. Device breakdown voltage exceeds 50 V at $I_{gd}$=1 mA/mm. Non-linear device models were extracted for 4x75 $\mu$m and 8x75 $\mu$m devices (number of gate fingers by gate width) at 10 GHz. To support supply modulation applications, the models were fit to S-parameter and load pull data measured at low drain current over a wide range of drain bias voltages. Load pull results for a PAE of 62% at 10 GHz and 20 V drain bias demonstrated 3.4 W/mm output power density with associated gain of 14 dB.

### B. Circuit Design

Various FET cell sizes from 8x50 $\mu$m to 12x100 $\mu$m were used to produce output powers of 2.5, 3, 4 and 10 W at 20 V drain bias. The designs maximize PAE over a range of drain biases, and therefore, the amplifiers do not operate as any specific PA class. Fig. 1 shows photographs of the fabricated MMICs which were designed as follows:

- Circuit B (Fig. 1a) is a 2-stage amplifier that combines four 10x90 $\mu$m transistors for the output stage. The driver stage utilizes two 8x50 $\mu$m FET cells and is biased in class-AB. The output stage is designed following a class-

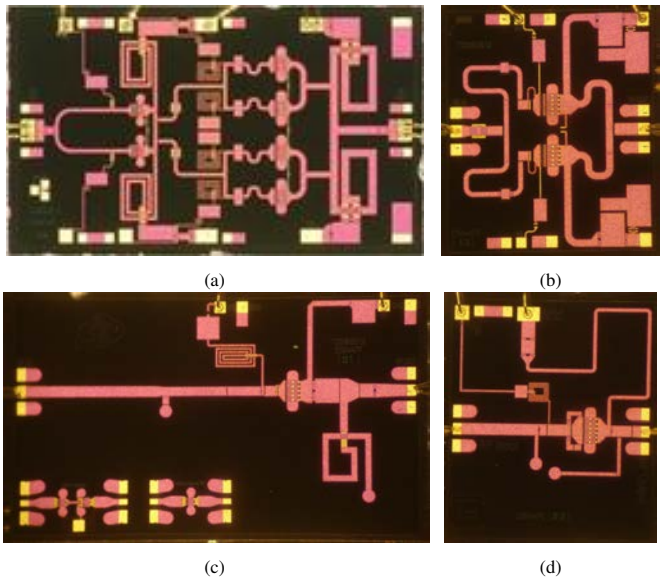

Fig. 1: (a) Circuit B: 2-Stage MMIC, output stage combines 4 10x90 $\mu$m. 3.8x2.3 mm$^2$ (b) Circuit D: Single stage, two 10x100 $\mu$m. 2.0x2.3 mm$^2$ (c) Circuit F: Single stage, 10x100 $\mu$m. 3.8x2.3 mm$^2$ (d) Circuit E: Single stage, 12x100 $\mu$m. 2.0x2.3 mm$^2$

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E approach for the highest $V_{ds}$. For lower drain biases, the PA is expected to operate in sub-optimal class-E.

- Circuit D is a single stage amplifier that combines two 10x100 $\mu$m transistors with a reactive combiner. The layout is shown in Fig. 1b.
- Circuit E uses a single 12x100 $\mu$m transistor in a class-$F^{-1}$ configuration. The layout is shown in Fig. 1d.
- Circuit F is a single stage amplifier using a 10x100 $\mu$m transistor. The layout shown in Fig. 1c includes test structures and has an unnecessarily long input network to fit the reticle layout of the wafer.

## III. Measured Results

During production, fabricated devices were tested on-wafer for output power and efficiency. Measured on-wafer results under 20 V pulsed drain bias conditions gave frequency response and output power as expected from simulations. For one of the single stage amplifiers, a constant 30 dBm input power level gave an output power of about 36.8 dBm with $\pm$0.5 dB variation over the $\sim$120 device sample from 3 wafers.

Separated die were soldered to 40 mil thick CuMo carrier plates. The amplifier input and output bond pads were connected to 10 mil thick alumina de-embedding lines with two short bond wires. The carrier assembly is then inserted into an aluminum test fixture. The opposite ends of the alumina de-embedding lines are contacted with connectorized launchers and the entire fixture is placed on an aluminum heat sink. A photograph of the fixture is shown in Fig. 2. The in-fixture measurements were performed under continuous wave (CW) conditions at room temperature.

The calibration procedure de-embeds the launchers and alumina lines up to the bondwire/alumina interface. This was performed by measuring the power difference without and with a 50 $\Omega$ alumina Thru line (mounted and connectorized the same way as the MMICs). The power difference was divided in half for each side of the alumina de-embedding line.

Measured results for RF output power, $P_{out}$, and PAE for the MMICs are plotted below in Figs. 3a and 3b respectively. The measured optimal frequency of operation is higher than the expected 10 GHz for all designs, attributed to the device model. The gate voltage and input power were optimized for a combination of PAE and output power. The measured output power for Circuit B at 20 V drain bias is 10-13 W over a 10-11 GHz frequency band and has an associated PAE from 51% to 60% over the same frequency range.

The input power sweeps versus PAE and drain voltage are shown for the two stage (Circuit B) and a single stage (Circuit E) amplifier versus output power in Figs. 4a and 4b. The efficiency is >48% for both circuits down to 10 V on the drain and for Circuit B, the PAE is >54% down to 7.5 V. This is equivalent to an 8 dB output power adjustment range with peak PAE above 50%. As expected, the sub-optimal class-E design of Circuit B maintains a high efficiency that is less sensitive to changes in supply voltage.

A summary of the measured parameters (the best combination of PAE and output power) for the MMICs are in

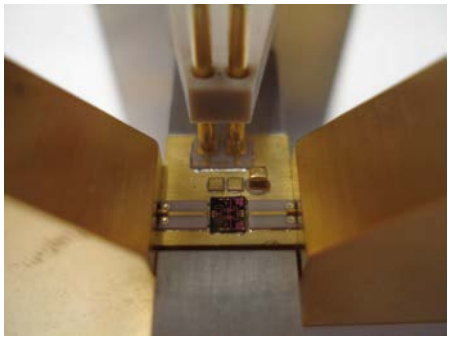
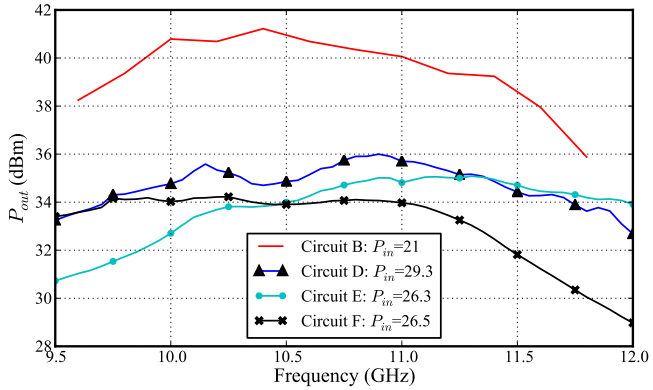
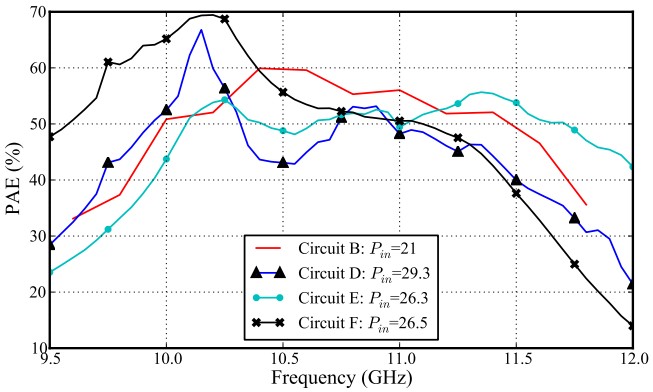


Fig. 2: Fixture used for measured results. The launchers contact the alumina with the coaxial center pin. For all MMICs, the gate bias pads on the MMIC are connected via a bondwire to a 1000 pF capacitor in parallel (gold squares above the MMIC). The drain pads are connected to a 1000 pF and an additional 0.01 $\mu$F capacitor. Circuit D is pictured (2.0x2.3 $mm^2$).




(a)




(b)

Fig. 3: Measured output power (a) and PAE (b) for the four MMICs over frequency. Each PA input power and quiescent bias current is selected for the best combined PAE and output power.

Table I. The output power versus supply voltage dependence is shown for the available measured data in Fig. 4 and the parameter $\Delta P_{out}$ and $\Delta V_{ds}$ for 50% PAE is calculated in the table. This metric describes the amount of power back-off and corresponding drain voltage achievable at 50% PAE. The measured watts per millimeter (using the output stage gate size) is approximately 3.6 W/mm (for the best design) for

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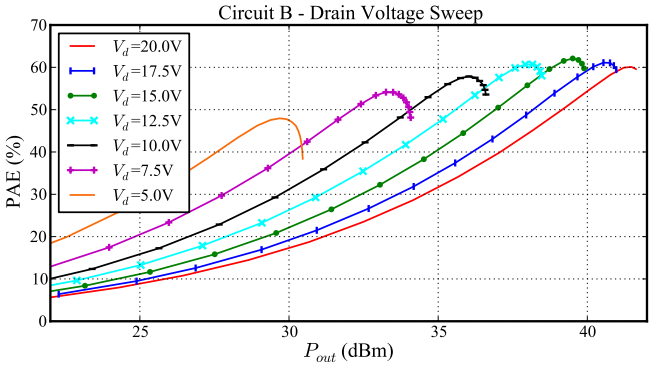
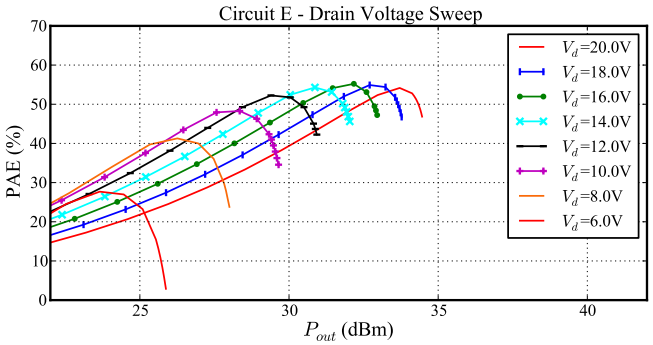



(a)




(b)

Fig. 4: Performance over supply voltage for the 2-stage MMIC, Circuit B (a) and single stage MMIC Circuit E (b). As the drain supply voltage is varied, both MMICs exhibit a PAE >50% with ∼5 dB output power variation.

this GaN process which is slightly higher than the modeled data from the 4x75 $\mu$m and 8x75 $\mu$m devices. Note that the model was extract from devices made in an previous version of the 0.15 $\mu$m process, and therefore we did not expect exact agreement with simulations. In addition, the transistors are operating close to a switched mode in all MMICs, and most nonlinear models will not accurately predict the performance. Nevertheless, the model used for these designs gave very good agreement with output and PAE.

## IV. Conclusion

The design and measured results for X-Band power amplifier MMICs that utilize 0.15 $\mu$m GaN on SiC process technology have been presented. Under continuous wave operating conditions these single and 2-stage MMICs demonstrated high efficiency (>50%) over large drain bias ranges (7.5-20 V) for supply modulated applications. For Circuit B, a 12.5 V reduction in supply voltage the output power is reduced 8 dB and the associated PAE is maintained at 54%. It is important to note that with the inclusion of a supply modulator, the linearity of the system will become worse, and will necessitate other means of linearization, including vector split schemes [6] and/or digital pre-distortion.

TABLE I: Measured MMIC Parameters

| Circuit | B | D | E | F |
|---|---|---|---|---|
| Max PAE (%) | 59.9 | 66.8 | 55.7 | 69.4 |
| Max $P_{out}$ (W) | 13.2 | 3.98 | 3.22 | 2.64 |
| Gate size (mm) | 3.6 | 2.0 | 1.2 | 1.0 |
| W/mm | 3.68 | 1.99 | 2.69 | 2.64 |
| BW at PAE=45% (GHz) | 1.6 | 0.77 | 1.88 | 1.95 |
| $\Delta P_{out}$ at PAE=50% (dB) | 11 | 3.3 | 4.8 | 5.3 |
| $\Delta V_{ds}$ at PAE=50% (V) | 12.5 | 7 | 9 | 8 |

## Acknowledgment

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