In-Package Harmonic Termination Design
for Improving Active Device Efficiency

Sushia Rahimizadeh*, Jérôme Chéron*, Qianli Mu†, Zoya Popović*

*Department of Electrical, Computer and Energy Engineering, University of Colorado, Boulder, CO, 80309-0425

†Infineon Technologies, Morgan Hill, California, 95037

Abstract—This paper discusses design of in-package reactances that can optimize efficiency of power amplifier transistors by specific and well-defined harmonic terminations and pre-matching within the device package. The methodology uses a passive fundamental-only load-pull tuner to characterize the transistor. As an example, the method is applied to a 10-W Infineon LDMOS device at a fundamental frequency of 2.6 GHz, by terminating the 5.2-GHz second harmonic using bond-wire and capacitor filters of various topologies. A 60% PAE is achieved with the method.

Index Terms—Transistor package, power amplifier, bond wire, harmonic load pull, LDMOS

I. INTRODUCTION

Packaged RF and microwave power transistors have additional reactances from the package, which limit the impedance range that can be presented to the intrinsic device. For example, the capacitance presented by a standard LDMOS package with 280-mil tab width is 5.6 pF, which corresponds to approximately $jX_C(4\,\text{GHz}) = -j7\,\Omega$ reactance at the second harmonic of a 2-GHz signal, effectively shorting the harmonics. Since high-efficiency classes of power amplifier operation depend on specific harmonic terminations at the device virtual drain (intrinsic current source), e.g. [1], this implies that the package prevents high-efficiency transistor operation. In addition, the package parasitics limit the range for the fundamental-frequency match. While this holds true for any active device, in this paper, LDMOS transistors will be addressed due to their low input/output impedance, larger parasitic reactances, and limited frequency of operation compared to GaN devices. The presented method is more general and can applied to any active device where harmonic network design is of interest, e.g. rectifiers [2].

The modeling of high-power transistor packages and the passive elements within them has been studied in [3], [4]. Similar simulation methods are used in this work to understand and design the transistor package environment in terms of both the fundamental and the 2nd harmonic. Fig.1 shows an example layout of the inside of a power device package, where the gate and drain manifolds on the die are bonded to a filter consisting of a shunt capacitor and a large number of bond-wires. This low-pass filter is connected to the package lead (tab) and acts as an impedance transformer that helps to a certain degree with the fundamental match, and is a standard approach in most packaged devices, e.g. [5]. Fig. 2a shows the circuit diagram, where the bond-wire inductance is on the order of 1 nH and defined by packaged size and device position, while the MOS capacitor values are chosen depending on device
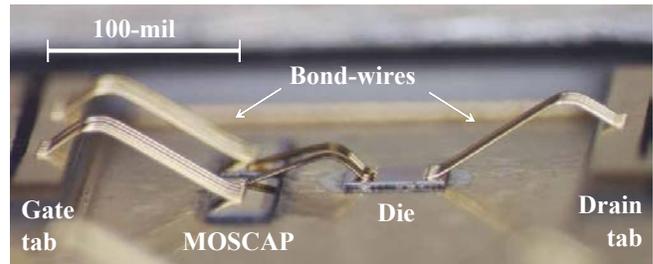

Fig. 1. Typical LDMOS power transistor package showing the bond-wires that connect the gate and drain manifolds to the package lead via a shunt MOS capacitor that, together with bond-wire inductance, provides pre-matching at the fundamental frequency.
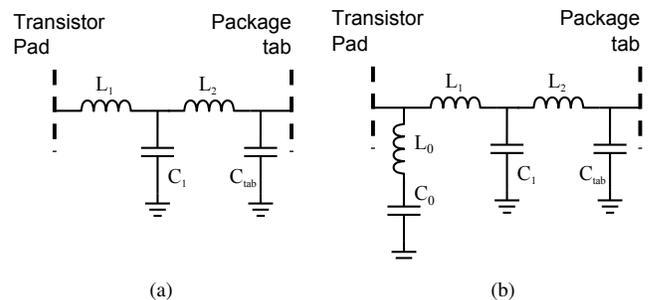

Fig. 2. Two filter topologies considered in the package design: (a) Single shunt capacitor and (b) higher-order topology in which C_0 and L_0 are used to terminate the second harmonic.

size. The tab capacitive reactance is now transformed through the Tee (LCL) network for better fundamental matching. This topology is shown to improve efficiency and bandwidth for GaN devices in [6], where the limited impedance range of the harmonic was sufficient. LDMOS devices present a more difficult challenge due to the extreme impedance values. Fig. 2b shows another possible in-package filter topology that can be implemented with bond-wires and MOS capacitors with enough degrees of freedom to improve the match at both fundamental and harmonic frequencies.

Experimental and simulated results will be shown for several packages specifically designed for fundamental load-pull to characterize a 10-W Infineon LDMOS device at the fundamental frequency of 2.6 GHz and its second harmonic. The methodology is illustrated with simulations in Fig. 3 using a non-linear device model from the manufacturer. The constant PAE contours show 2nd harmonic impedances with the fundamental fixed at the impedance found by fundamental
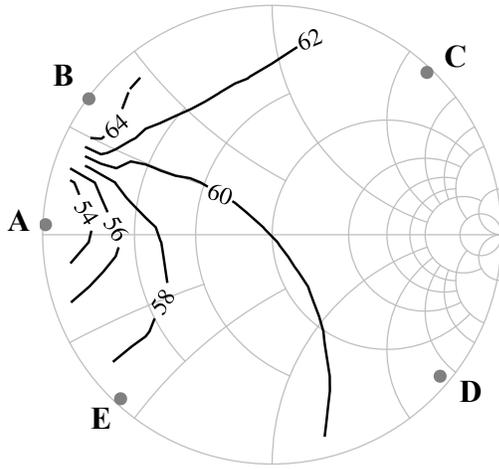
Fig. 3. Simulated PAE load-pull contours at $2f_0$, at the die reference plane. The $2f_0$ terminations for each of the 5 package designs are indicated by the grey dots.

load pull ($Z(f_0) = 3.4 + j12.7\,\Omega$). Five packages were then designed (A-E) with the same fundamental pre-match but each with a different 2nd harmonic impedance, terminated strategically and diversely around the Smith chart.

TABLE I
CIRCUIT MODEL ELEMENT VALUES FOR EACH DESIGN

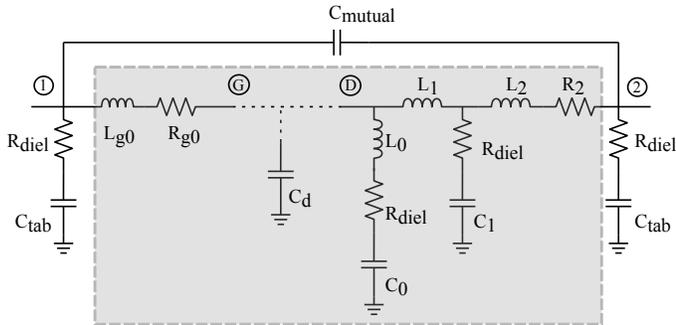| Element	Package Design				
	A	B	C	D	E
L_0	1.2 nH	2.0 nH	1.0 nH	0.4 nH	0.7 nH
C_0	0.78 pF	0.78 pF	0.32 pF	0.64 pF	0.93 pF
L_{g0}	L_2	L_1	C_1	C_{tab}	C_{mutual}
0.8 nH	1.5 nH	1.5 nH	7.11 pF	5.6 pF	0.1 pF

Fig. 4. Equivalent circuit for the 10-W device package with in-package matching. The dashed-line box encapsulates the bond-wire and capacitor elements which were designed. The significant parasitics are reflected in the model. The gate and drain die pads are indicated by G and D, and the capacitor C_d is inserted in the package in place of the die for experimental model validation.

The remainder of the paper discusses first the package choice and pre-matching fixture design for obtaining load-pull information that validates in-package filter effect on efficiency. Next, in-package filter design based on bond-wires
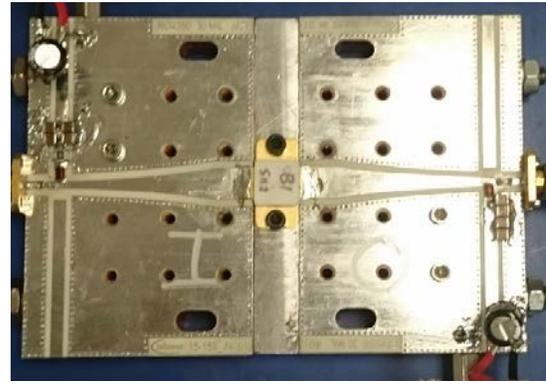

Fig. 5. Load-pull fixtures used to mount the package and exponentially taper $50\,\Omega$ lines to the 280-mil wide lead of the packages. A bias tee is integrated with the taper, with a $10\,\Omega$ resistor on the gate bias for stability.

and capacitors is presented for both input and output networks. Finally, load-pull measurements are compared to simulations and a path to package design for high-efficiency operation is discussed.

II. IN-PACKAGE DESIGN AND VALIDATION APPROACH

Among the various standard packages available from the manufacturer, a package was chosen with dimensions able to support higher-order filter designs (but not so large as to force long bond-wires which would lead to increased loss), and with tab widths as small as possible to reduce package parasitics. The chosen package is simulated in Ansys HFSS to determine the package parasitic elements shown outside the dashed-line in Fig. 4. The given package is seen to have a parasitic capacitance due to the package tabs of 5.6 pF at both the gate and drain. The package also exhibits a mutual capacitance between the package leads of 0.1 pF which proves to have an impact on the S_{21} at the harmonics and therefore must be considered in the design of terminations. Dielectric loss, R_{diel} of $0.2\,\Omega$ is seen in the MOS capacitors. The elements shown within the dashed-line box are then designed with the package parasitics, with knowledge of the fundamental and harmonic load and source-pull device impedances obtained from the device model. To obtain impedances given by points A through E in Fig. 3, the values of the circuit model are chosen within realizable values of bond-wire inductances (0.2 to 3 nH) and available MOS capacitors (0.24 to 8 pF) for both gate and drain in-package networks.

The package designs require iteration between full-wave, passive circuit, and harmonic balance simulations with the non-linear device model until the desired impedances at both the fundamental and 2nd harmonic is achieved. The circuit model parameter values for the final, manufacturable, in-package networks are listed in Table 1. The networks are designed such that L_0 and C_0 can be tuned for each harmonic termination while the rest of the elements remained constant for each design to maintain a similar fundamental pre-match.

In order to determine the accuracy of the fabricated packages to the desired, a passive version of each package (A
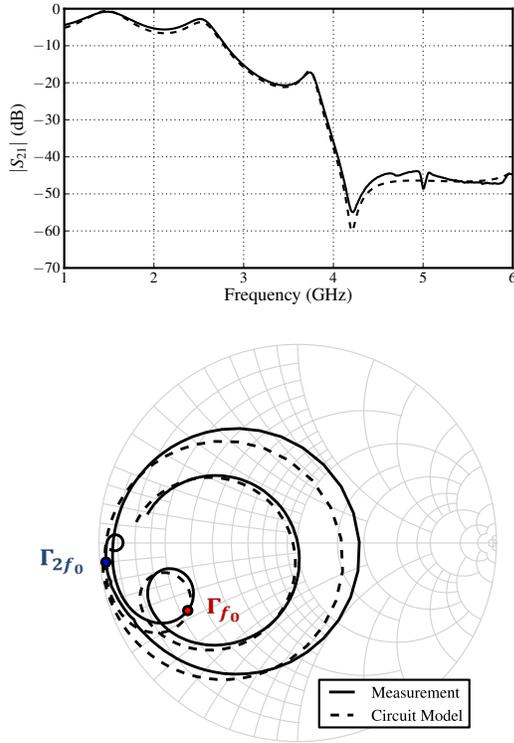
Fig. 6. Measured (solid line) vs. simulated (dashed line) S-parameters of the equivalent package circuit from Fig.4: (top) transmission coefficient magnitude and (bottom) magnitude and phase of S_{11} from 1 to 6 GHz.

through E) is designed in which the transistor was replaced by a shunt capacitor of similar size and known capacitance ($C_d = 2.58 \, \text{pF}$). This allows S-parameter measurement and comparison to HFSS simulations at the same reference plane. TRL calibration was performed to de-embed the measurement plane to the package frame. A circuit model is then fit to the de-embedded S-parameter measurements. Validation measurements are performed using a pre-matching fixture shown in Fig.5, where exponentially-tapered microstrip lines on a Rogers 4350B 30-mil substrate transform 50-Ω to the $17 \, \Omega$ characteristic impedance of the package tab at the package reference plane. Fig. 6 shows the resulting measured vs. predicted performance for one of the 5 packages from 1 GHz to above the second harmonic. The $|S_{21}|$ shows the expected low-pass filter behavior as well as the termination at 5.2 GHz. Similar agreement is obtained for all 5 packages, validating the approach.

III. Measurements with Transistor in Package

After validating with the passive packages, the 5 harmonic termination designs (A - E) are populated with 10-W LD-MOS die, and a fundamental load-pull is performed with the packaged devices mounted in the fixture from Fig. 5. The packages designs showing positions of bond-wires and capacitors relative to the 10-W die are shown in Fig. 7.

Fundamental load-pull was performed for all of the designs, and an example for package design B is shown in Fig. 8. The
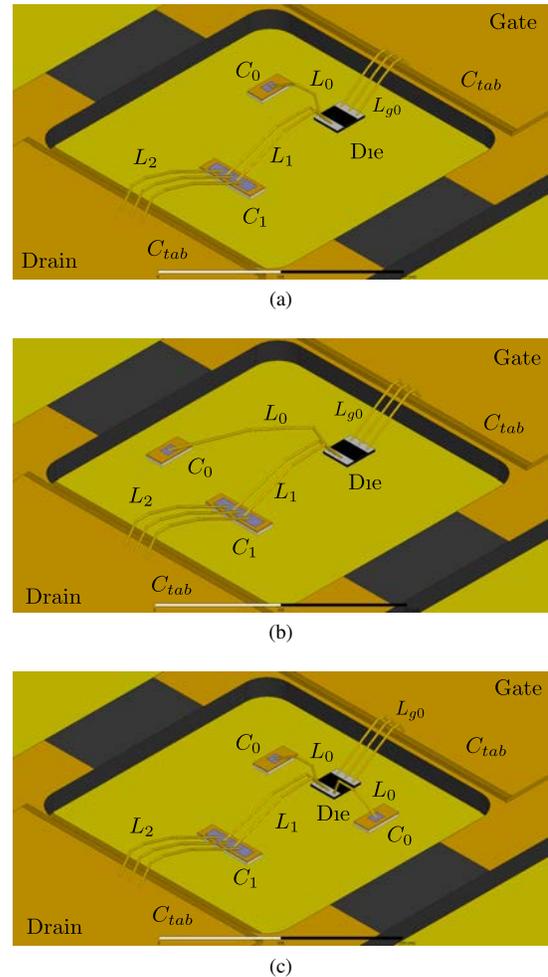

Fig. 7. Matching networks from Table 1 realized within a package. Three distinct packages networks are shown, with varying element values: (a) designs A and C, (c) design B, and (b) designs D and E.

tuner impedance constellation is shown in two sets of dots, one set at the package reference plane and the other at the die plane. The maximum simulated and measured PAE points are shown with a red and blue cross symbol, respectively. The agreement with simulation validates measurement and calibration, package design and fabrication, and the active device model.

Finally, Fig. 9 presents measured efficiencies for the various package designs that correspond to different second harmonic terminations. The fundamental impedance is also shown, and as expected, this impedance does not vary significantly, while the harmonic impedance moves around the edge of the Smith chart. The resulting PAE varies largely (by up to 15%) while the fundamental load remains the same, showing the dramatic effect of in-package harmonic termination on PA efficiency.

For comparison, load-pull is performed on one side of a commercially available, push-pull packaged transistor from Infineon (PTFC260202FC), which houses the aforementioned device and a gate/drain fundamental pre-match. Similar to the previously described load-pull, fundamental-only tuners
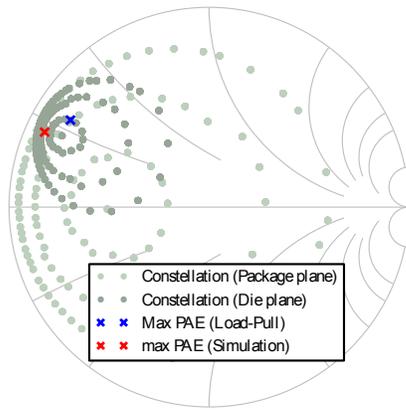
Fig. 8. Comparison between measured and simulated load-pull impedances at different reference planes showing the die reference plane and package reference plane, for package design B.
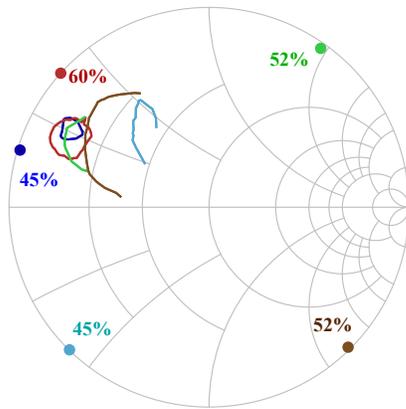

Fig. 9. Fundamental frequency constant drain efficiency contours measured at each 2nd harmonic termination, referenced at the die plane. Maximum efficiency of each contour is indicated next to the corresponding harmonic termination dot.
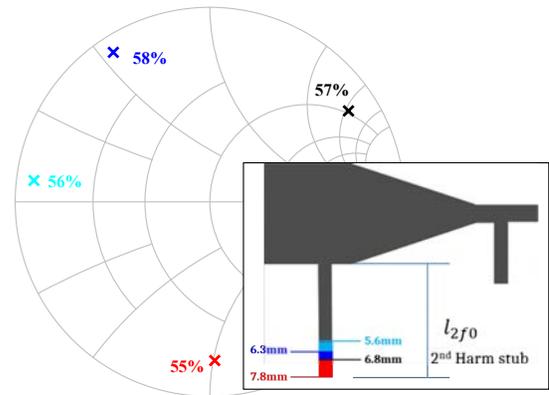

Fig. 10. Maximum efficiencies found with fundamental load-pull iterated at 4 discrete 2nd harmonic impedances (indicated by crosses). The colors correspond to the 4 relative lengths of an open-circuit stub used to control the 2nd harmonic on the load-pull fixture, external to the package.

were used. However in this case, the 2nd harmonic was tuned external to the package by varying the length of a microstrip open-circuit stub on the load-pull fixture, as done in [2]. Although the maximum efficiency is similar in both cases, it was seen that PAE is more sensitive to the 2nd harmonic impedance in the in-package design, indicating a greater command of the 2nd harmonic.

IV. CONCLUSION

An LDMOS transistor is characterized using a fundamental-only tuner and various 2nd harmonic terminations. Two methods of harmonic tuning are compared, differentiated by the reference plane at which they are tuned, to demonstrate increased harmonic sensitivity and the efficacy of in-packing matching. Package parasitics, traditionally an efficiency-inhibiting factor, are used to the advantage of the matching network at a larger range of frequencies than just the fundamental. The package and the package-internal passives are modeled beyond the 2nd harmonic in full-wave simulation and validated in measurement by fully passive versions of the package designs, allowing the design of an in-package harmonically-terminated transistor.

The described technique enables greater harmonic control of an LDMOS-based PA at a 2.6 GHz, pushing the frequency limit of high-efficiency operation in a technology with characteristically difficult intrinsic and extrinsic impedances in terms of harmonic control. The methodology can be extended to the design of more complex classes of operation which rely on effective termination of harmonics, such as Class-F/F^{-1} power amplifiers.

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