SECOND EXAM
ECEN 2120 - Lecture 1
November 7, 2008

This exam is closed book and closed notes. You may use a calculator.

Write your name on every page. Please sign the honor code statement below. Read through the entire exam, and then answer all the questions. Do all your work on the exam itself -- if necessary, turn the page over or use the back of the previous page. For multiple choice questions, clearly circle your answer. You have 50 minutes. Good Luck!

On my honor, as a University of Colorado at Boulder student, I have neither given nor received unauthorized assistance on this test.

Signature: __________________________________________________________

Question 1. (7 points) A circular buffer of length 1024 is being implemented. This buffer holds 8-bit characters. To access the buffer, the label INBUFF points to the base of the buffer and an inptr and outptr are used as offsets from the base. The inptr and outptr may be referenced with the labels IPTR and OPTR, respectively and both are defined as long words. Write an efficient sequence of assembly code to update the IPTR when a character is inserted into the buffer. (Don’t worry about checking for overflow or overwrites.)

Question 2. (4 points) What is the name of the multi-programming strategy where a timer interrupt may cause the scheduler to stop a process from running and start a different process?

Question 3. (4 points) To help support mutual exclusion for processes, instructions are added to an architecture. Based on our discussion in class, which of the following are such instructions?

(a) EXCH  (b) CMPI  (c) ADDQ  (d) TAS  (e) a and d.
Question 4. (5 points) A system has four devices connected to it. Devices X and Y are connected in a daisy chain to the level 6 priority line of a PIC, with X closer to the PIC than Y. Devices A and B are connected to the level 4 priority line of the PIC, with A closer to the PIC. Assume everything is properly enabled and the interrupt service routines are properly written and will not allow devices to interrupt them. If all four devices simultaneously want to interrupt the CPU, what is the order in which the devices will be serviced? (Assume 68000 priority levels.)

(a) B, A, Y, X  
(b) X, A, Y, B  
(c) X, Y, A, B  
(d) Y, X, B, A  
(e) A, B, X, Y  
(f) A, X, B, Y  
(g) None of these.

Question 5. (5 points) An assembly code sequence correctly implements a P operation on a binary semaphore named Flag. Which of the following statements is true?

(a) The P operation increments Flag.
(b) The P operation is executed before entering a critical section.
(c) The semaphore is a 1 when a process is in the critical section.
(d) The P operation supports mutual blocking.
(e) b and c are true.

Question 6. (5 points) Consider the following macro definition:

```
ThisMacro macro A,B,C
    local base
    base set *
    ds.w A
    L1 set *-base
    dc.l B
    L2 set *-base
    dc.w C
endm
```

When this macro is called with the string "ThatMacro ThisMacro 20,D,10", what is the value of the label L1?

(a) 0  
(b) 2  
(c) 20  
(d) 40  
(e) ThatMacro + 2

Question 7. (4 points) A sequence of code requires 40 cycles to execute on a 3.2 GHz processor. How much time does it take for the sequence to execute?

Question 8. (4 points) When discussing the RS-232 standard, which of the following signals is a "handshake" for DSR?

(a) RD  
(b) DTR  
(c) RI  
(d) CTS  
(e) b and d are used.
Questions 9-10. For the following two questions, D0 initially contains the value $22. The instruction BSET #4,D0 is then executed.

Question 9. (5 points) What is the value in D0 after the instruction has executed?
(a) $04  (b) $26  (c) $2A  (d) $32  (e) None of these.

Question 10. (3 points) What is the value of the Z bit in the SR after the instruction has executed?
(a) 0  (b) 1  (c) Not enough information.

Questions 11-14. Consider a UART running at 9600 baud. This system is set-up to use 1 stop bit, 8 data bits and odd parity. The line is normally held at a logical "1". Assume that the character "u" ($75) is to be transmitted on the line.

Question 11. (3 points) What is the value of the parity bit?
(a) 0  (b) 1  (c) Not enough information.

Question 12. (4 points) At most, how many data items (characters) can be transmitted per second?
(a) 872  (b) 960  (c) 1066  (d) 1200  (e) 9600

Question 13. (5 points) The frame that represents the transmission of the "u" is (from first bit sent on the left to last bit sent on the right, where the "P" represents the value of the parity bit):
(a) 01010110P1  (b) 011101010P1  (c) 01010111P1  (d) 01110101P1  (e) 1110101P1

Question 14. (5 points) For the serial line described above, assume the following frame is sent to a receiver (again reading from the first bit sent on the left to last bit sent on the right):
01011001101
The receiving UART has its baud rate set at 19200 baud. What will happen?
(a) The receiver would appear to receive two characters, but not the character sent.
(b) The receiver would receive the original character sent.
(c) A parity error would occur.
(d) A framing error would occur.
(e) Both a parity and a framing error would occur.

Question 15. (3 points) When using the UART, which of the following would be considered a control register:
(a) IIR  (b) MSR  (c) LCR  (d) a and c  (e) All are control registers.
Questions 16-17. Consider the MB5 68000 system that you have been using and an interrupt handler associated with the level 5 interrupt autovector. The name of this new interrupt handler is MyHandler and the linker has assigned it to be at location $1070C0.

Question 16. (5 points) After the processor acknowledges an interrupt, in which range of addresses given below does the processor find the first instruction it executes.

(a) $0-$3FF  
(b) $100000-$100200  
(c) $105000-$109000  
(d) $1FF000-$1FFFFF  
(e) None of these.

Question 17. (3 points) From the point of view of what the hardware does, the only difference between invoking MyHandler and executing a JSR instruction is that the target address comes from the interrupt vector rather than from an addressing mode used in the instruction.

(a) True  
(b) False

Question 18. (3 points) When discussing the RS-232 standard, it was pointed-out that only three signal lines are needed to make a connection between a computer and a terminal. Which of the following would be used?

(a) TD  
(b) CTS  
(c) DSR  
(d) DTR  
(e) a and d.

Questions 19-20. Assume that you are dealing with the simple multi-processing system described in class.

Question 19. (4 points) Where is process state information stored?

Question 20. (3 points) A process waiting for I/O is in which state?

Question 21. (4 points) What is the name of the technique whereby a DMA controller uses idle bus cycles to perform its data transfers?

Question 22. (3 points) The value of MBIT is a mask that is set with an EQU. Which of the following lines of code would set bits in D0 according to the position of 1’s in MBIT, without modifying the rest of the bits in D0.

(a) AND.L #MBIT,D0  
(b) BSET #MBIT,D0  
(c) OR.L #MBIT,D0  
(d) OR.L MBIT,D0  
(e) None of these.
Question 23. (5 points) One way to debug your interrupt handler code was to write to the LEDs. The following line of code was written to do this.

```assembly
move.l #1,$B00001
```

When the code executes, what will happen?

(a) The right-most LED will be on and the others will be off.
(b) The right-most LED will be off and the others will be on.
(c) The right-most LED will be off and the others will be the way they were before the instruction was executed.
(d) A line 1010 emulation error will occur.
(e) An address error will occur.

Question 24. (4 points) Consider the following instruction:

```assembly
bset.b D0,-(A0)
```

How many machine cycles does it take for this instruction to execute?

Some useful information.

Table D-1. Effective Address Calculation Times

<table>
<thead>
<tr>
<th>Addressing Mode</th>
<th>Byte Word</th>
<th>Long Word</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dn</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>An</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(An)</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>(An)+</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>-(An)</td>
<td>6</td>
<td>10</td>
</tr>
<tr>
<td>d(An)</td>
<td>8</td>
<td>12</td>
</tr>
<tr>
<td>d(An,X)</td>
<td>10</td>
<td>14</td>
</tr>
<tr>
<td>xxx.W</td>
<td>8</td>
<td>12</td>
</tr>
<tr>
<td>xxx.L</td>
<td>12</td>
<td>16</td>
</tr>
<tr>
<td>d(PC)</td>
<td>8</td>
<td>12</td>
</tr>
<tr>
<td>d(PC,X)</td>
<td>10</td>
<td>14</td>
</tr>
<tr>
<td>#xxx</td>
<td>4</td>
<td>8</td>
</tr>
</tbody>
</table>

Table D-8. Single Instruction Execution Times.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Dynamic</th>
<th>Static</th>
</tr>
</thead>
<tbody>
<tr>
<td>BSET</td>
<td>8+</td>
<td>12+</td>
</tr>
</tbody>
</table>

+ add effective address calculation time