ECEN 2120: Practice for Midterm Exam 2
Prof. Aaron Bradley, November 6, 2009

The following practice exam is similar to the exam that you will take in class on Wednesday, November 11. The exam is closed: notes, books, and electronic equipment (including calculators) are prohibited.

1. Which of the following sequences of code does **not** result in `(a0) = $B00001`?

   (a)
   ```
   ADDR    dc.l    $B00001
           ...
           move.l  ADDR,a0
   ```

   (b)
   ```
   ADDR    dc.l    $B00001
           ...
           lea     ADDR,a0
           move.l  (a0),a0
   ```

   (c)
   ```
   ADDR    equ     $B00001
           ...
           lea     ADDR,a0
   ```

   (d)
   ```
   ADDR    equ     $B00001
           ...
           move.l  #ADDR,a0
   ```

   (e) None of the above.

2. Consider the following code snippet:

   ```
   N       equ     256
           ...
           move.b  #N,d0
   LOOP    move.w  (a0)+,(a1)+
           subi.w  #1,d0
           bne     LOOP
   ```

   How many times does `(PC) = LOOP`?

   (a) 0 times

   (b) 1 time

   (c) 255 times

   (d) 256 times

   (e) The number of times cannot be determined from the given information.

For the following three questions, consider the following code snippet:

```
DEV_W   equ     $B00001         ; LEDs                          (1)
TABLE   ds.w    8                                               (2)
        ...
        lea     TABLE,a0                                        (4)
        move.l  DEV_W,a1                                        (5)
        move.b  #7,d0                                           (6)
* Write the lower byte of each entry in TABLE.
LOOP    move.b  (a0)+,(a1)                                      (7)
        jsr     pause                                           (8)
        dbf     d0,LOOP                                         (9)
```

3. Which line (probably) causes a memory error when this code is executed on the MB5?

   (a) (4)

   (b) (5)

   (c) (7)

4. Assuming the memory error is fixed, which line causes the loop to run longer than expected?

   (a) (4)

   (b) (5)

   (c) (6)

   (d) (7)

   (e) (9)

5. Assuming both of the previous two errors are fixed, which line causes the wrong data to be displayed?

   (a) (2)

   (b) (6)

   (c) (7)

   (d) (9)

For the following two questions, suppose that two UARTs are initialized to communicate at 28800 baud and use eight (8) data bits, one (1) stop bit, and odd parity.

6. Assuming that there is no delay between sending/receiving each character, how many characters can be communicated per second at most?

   (a) fewer than 2880 characters

   (b) 2880 characters

   (c) greater than 2880 characters

7. Suppose that the ASCII character '`x`', with ASCII code `$78`, is written to the sending UART. Which of the following, read left to right, represents the frame with that data that is sent over the communication medium?

   (a) `10001111010`

   (b) `000011110111`

   (c) `00001111001`

   (d) `00001111011`

   (e) `0000111111`

8. Which error can result if the UART device software is not diligent about reading data from port RBR when it is there?

   (a) Parity error

   (b) Overrun error

   (c) Underrun error

   (d) Framing error

   (e) No error results, but data may be lost

9. Consider a circular buffer whose total data section has two bytes, and the following sequence of puts and gets:

```
n = 0;
while(1) {
  put(n); n++;
  put(n); n++;
  printf("%d\n", get(n));
}
```

   Which sequence of numbers are printed?

   (a) 0, 1, 2, 3, ...

   (b) 0, 2, 4, 8, ...

   (c) 0, 3, 4, 7, ...

   (d) 1, 3, 5, 7, ...

   (e) None of these.

10. Consider a circular buffer whose total data section has three bytes and the following sequence of puts and gets:

```
n = 0;
while(1) {
  put(n); n++;
  put(n); n++;
  printf("%d\n", get(n));
}
```

Which sequence of numbers are printed?

(a) 0, 1, 2, 3, 4, ...

(b) 1, 2, 3, 5, 7, ...

(c) 0, 1, 2, 4, 6, ...

(d) 0, 3, 4, 7, 8, ...

(e) None of these.

11. In the read/write bus protocol, what allows the CPU to wait an arbitrarily long time for a device to assert the data on the bus.

(a) The CPU waits for the signal to stabilize on the data bus.

(b) The device asserts $\overline{\text{DTACK}}$.

(c) The device deasserts the address bus.

(d) The CPU asserts $\overline{\text{DTACK}}$ and waits for the device to deassert it.

(e) None of the above, as the read/write protocol must fit within four CPU cycles.

12. Consider the following sequence of code executed on a board in the lab:

```
lea     TABLE,a0
move.b  (a0,d1.w),(a0,d2.w)
move.b  #%00000010,#$B00001
```

How many times does data travel on the system bus?

(a) 0 times

(b) 1 time

(c) 2 times

(d) 3 times

(e) 4 times

13. A device's capacity for Direct Memory Access (DMA) is only useful if

(a) there is another device that also has DMA capability.

(b) the data bus is at least 16 bits.

(c) the applications on the system are I/O- but not CPU-intensive.

(d) the CPU is capable of performing bus arbitration.

(e) (c) and (d)

For the following two questions, suppose that a 1 GHz CPU executes a tight loop that requires 20 cycles and that proceeds through 500 equally-spaced samples of a sine wave 100 times, writing each sample to a D/A converter.

14. Which frequency of sound is produced?

    (a) 1 KHz

    (b) 100 KHz

    (c) 1 MHz

    (d) 100 MHz

    (e) None of the above.

    (Bonus: Which is more likely to hear it: an elephant or a bat?)

15. How long is the sound pulse?

    (a) .1 millisecond

    (b) 5 milliseconds

    (c) 10 milliseconds

    (d) 100 microseconds

    (e) None of the above.

16. Suppose that a clock has a frequency of 10 MHz and that you want to produce a tone with frequency 10 KHz by proceeding through 20 equally-spaced samples of a sine wave many times. To what should you set the counter?

    (a) 1000

    (b) 500

    (c) 100

    (d) 50

    (e) None of the above.

17. Consider the following sequence of acquisitions of locks:

```
acquire(lock1);
acquire(lock2);
acquire(lock3);
```

Assuming that the following sequences of acquisitions/releases are executed in another thread, which of the following can result in deadlock?

(a)
```
acquire(lock1);
acquire(lock3);
```

(b)
```
acquire(lock2);
acquire(lock3);
release(lock1);
```

(c)
```
acquire(lock1);
acquire(lock3);
release(lock3);
acquire(lock2);
```

(d)
```
acquire(lock2);
acquire(lock3);
release(lock2);
acquire(lock1);
```

(e) None of the above.

18. Consider the blocking buffer implemented with semaphores. What is the value of the shared variable `x` when both of the following processes are in the *blocked* state, assuming that the shared buffer `b` is initally empty?

```
Process 1                          Process 2

put(b, 0);                         x = get(b);
put(b, 1);                         x = get(b);
x = -1;                            x = -1;
get(b);                            get(b);
```

(a) 1

(b) -1

(c) Either 0 or 1, but not -1.

(d) Either -1 or 0, but not 1.

(e) Any of -1, 0, or 1.

19. The process state of *blocked* was introduced to optimize the use of which resource primarily?

(a) the CPU

(b) the system bus

(c) main memory

(d) the hard drive

(e) the operating system

20. Interpret the following 32 bits as an IEEE single-precision floating point number:

    `11000000111000000000000000000000`

    What is its decimal equivalent?

    (a) -.75

    (b) -0.35

    (c) -3.5

    (d) -7

    (e) None of the above.

21. Consider the decimal number 17.1. Choose the best approximation to 17.1 as a binary word in 8-bit fixed-point arithmetic (that is, 8 binary digits to the right of the radix point):

    (a) `$1118`

    (b) `$1111`

    (c) `$111C`

    (d) `$1718`

    (e) None of the above.

22. Consider the following scenario. UART1 should receive data that originates from the keyboard attached to the computer; UART2 should transmit these data to a terminal. Additionally, the D/A converter should broadcast the subset of the data that are ASCII characters 'a'-'z' or 'A'-'Z' or ' '. Finally, the LEDs should broadcast the data. Considering CPU usage and device limitations, the best choices for the form of I/O to use for each device are

    (a) UART1: interrupt; UART2: polled; D/A: unconditional; LEDs: unconditional

    (b) UART1: interrupt; UART2: interrupt; D/A: unconditional with clock-based interrupt; LEDs: unconditional

    (c) UART1: interrupt; UART2: polled; D/A: unconditional with clock-based interrupt; LEDs: unconditional

    (d) UART1: polled; UART2: polled; D/A: unconditional with clock-based interrupt; LEDs: polled

    (e) UART1: interrupt; UART2: polled; D/A: unconditional with clock-based interrupt; LEDs: polled

For the following two questions, consider the following page table for an 8-bit address virtual memory space mapped onto 128 bytes of physical memory:

7	00	0
6	01	1
5	00	0
4	00	0
3	10	1
2	11	1
1	00	1
0	00	0

23. Which virtual address is decoded as physical address `1011011`?

    (a) `10111011`

    (b) `11011011`

    (c) `01011011`

    (d) `11111011`

    (e) None of the above.

24. What happens upon executing the following instruction?

```
move.b  %11010010,d0
```

    (a) It is translated to physical address `1110010`, and the byte at that address is moved into `d0`.

    (b) A page fault occurs, and the operating system writes out page frame 6 to disk and writes in page 2 as page frame 6.

    (c) A page fault occurs, and the operating system writes out some page frame x to disk and writes in page 6 as page frame x.

    (d) A segmentation fault occurs as the address is beyond the range of physical memory.

    (e) A bus error ocurrs for no apparent reason.

25. The CUDA memory model consists of

    (a) grids of blocks of threads.

    (b) on-chip memory, device DRAM, and general DRAM.

    (c) per-thread registers and local memory, per-block shared memory, and per-grid global memory.

    (d) two levels of on-chip cache and device DRAM.

    (e) multiple SIMD cores.

26. How does CUDA's `__syncthreads()` prevent a race condition?

    (a) It ensures mutual exclusion of the critical sections.

    (b) No thread in a block can advance beyond it until all other threads in the block have reached it.

    (c) No thread can access shared memory between two invocations.

    (d) It forces threads to run sequentially subsequent to its execution.

    (e) No thread in a block can advance beyond it.

27. One can generally characterize devices as follows:

    (a) Devices are fiendishly clever instruments of torture and should be outlawed by international political bodies.

    (b) They can have ports that one writes to control the device and one reads to learn about its state, and data ports that one reads or writes to transfer data.

    (c) They can have control ports to which one writes to control their mode, status ports that one reads to determine their state, and data ports that one might read or write, though not necessarily both, to transfer data.

    (d) (b) or (c), depending on whether one is looking at the physical specification or high-level abstraction.

    (e) Devices are devices.