

Appendix C

From CDR Process to HiP Process

Competitive designs for wireless infrastructure applications require faster digital signal processors (DSPs) with reduced power requirements. To meet this industry demand, Motorola's roadmap for future DSP56300 family derivatives includes the application of continuously evolving, cutting-edge fabrication process technologies. This appendix describes the general differences between DSP56300 family derivatives that use Motorola's Communication Design Rules (CDR) process technology and derivatives that use Motorola's High-Performance (HiP) process technology. It presents the hardware and software design implications for DSP56300 family derivatives. Migration of DSP56300 family members from the CDR to the HiP4 process affects internal memory block size, voltage, operating frequency, and Port A timings. **Table C-1** summarizes the process-related differences for DSP56300 family derivatives using the CDR and HiP4 process technologies and identifies related trends for future process technologies. The remainder of this appendix discusses the differences summarized here.

Table C-1. CDR-to-HiP Process Differences Summary

Feature	CDR	HiP4	Future
Voltage	2.5 and 3.3v (core and internal PLL)	1.8v (core and internal PLL)	< 1.8v
Operating Frequency	100 MHz (maximum frequency)	Operating frequencies > 100 MHz	Operating frequencies >>100 MHz
Port A Timings:			
DRAM Access Support	Supported up to 100 MHz	TBD	TBD
SRAM Timings	Supported up to 100 MHz	Supported, but with additional wait states	Accesses may require additional wait states
Synchronous Timings	Referenced to CLKOUT	CLKOUT not supported	CLKOUT not supported
Arbitration Timings	Referenced to CLKOUT	CLKOUT not supported; alternatives exist	CLKOUT not supported; alternatives may continue to exist
Address Trace Mode	Supported	Not supported due to BCLK not functioning	TBD
Memory Block Size	256 x 24-bit words	1024 x 24-bit words	TBD
TBD = To be determined			

C.1 Voltage

DSP56300 family members are dual-voltage devices. The core and internal PLL of derivatives migrating to the HiP4 process technology operate from a 1.8v supply compared to the core and internal PLL of derivatives using CDR process technology, which operate from a 2.5v and 3.3v supply. The input/output pins on each device operate from an independent 3.3v supply. DSPs with split power supplies afford designers greater flexibility in migrating board designs to devices with new process technologies. Motorola's HiP process technologies will continue to take advantage of this feature.

C.2 Operating Frequency

DSP56300 family derivatives that use the CDR process technology operate at a maximum frequency of 100 MHz. HiP4 derivatives operate at frequencies greater than 100 MHz. As process technologies evolve, even greater speeds are anticipated.

C.3 Port A Timings

Speed increases resulting from the application of new process technologies affect all Port A timings as follows:

- DRAM Access Support

DRAM accesses are supported with DSP56300 family derivatives that use the CDR process technology at speeds up to 100 MHz. Support for DRAM access in HiP4 and beyond is being investigated.

- SRAM Timings

SRAM accesses are supported with DSP56300 family derivatives that use the CDR process technology at speeds up to 100 MHz. The application of the HiP4 process technology to the DSP56300 family results in additional wait states for SRAM timings. Future changes in process technology may continue to result in additional wait states.

- Synchronous Timings and Arbitration Timings

DSP56300 family members that use the CDR process technology rely on CLKOUT as a reference signal for synchronous timings and arbitration timings. The CLKOUT output pin provides a 50 percent duty cycle output clock synchronized to the internal processor clock when the Phase Lock Loop (PLL) is enabled and locked. At speeds made possible by HiP4 process technology, CLKOUT produces a low-amplitude waveform that is not usable externally by other devices.

Alternatives to using CLKOUT exist. One example is the use of the Asynchronous Bus Arbitration Enable Bit (ABE) in the Operating Mode register. When set, the ABE bit eliminates the setup and hold time requirements with respect to CLKOUT for \overline{BB} and \overline{BG} . Future changes in process technology may continue to produce alternatives to CLKOUT.

■ Address Trace Mode

Address Trace mode, when available and enabled by setting the ATE bit in the Operating Mode register of DSP56300 family derivatives that use the CDR process technology, allows users to determine the address of internal memory accesses. Specifically, when ATE is set, BCLK serves as a sampling signal and results in output of the memory access address on the address lines. With the application of HiP4 process technology, BCLK does not function. Without BCLK functioning, no signal exists to initiate the sampling process, and the DSP does not output any addresses. Therefore, Address Trace mode is not supported under the HiP4 process.

C.4 Memory Block Size

The internal memory block size of DSP56300 derivatives using the HiP4 process technology is 1024 x 24-bit words compared to 256 x 24-bit words in CDR derivatives. This change in size affects DMA/core contention (and EFCOP/core contention for derivatives, such as the DSP56307, that have an enhanced filter coprocessor).

In CDR derivatives, the internal RAM is divided into 256-word blocks. A situation of contention exists if the core and DMA access the same block of 256 words. If both the core and DMA access the same block, then the core always has priority, and the DMA is delayed until a free slot is available. If the core and DMA access different blocks, they do not interfere with one another; each continues to operate at its maximum speed. Memory block boundaries are located at 256 word addresses.

This same situation applies to HiP4 derivatives, except that contention exists if the core and DMA access the same block of 1024 words. Memory block boundaries are located at 1 K word addresses. To avoid DMA/core contention, DMA and core accesses must address different 1024-word blocks. The following figure shows two examples of core and DMA accesses to different 256-word blocks in the DSP56307 (no contention) and the resulting effect of these same accesses in a hypothetical HiP4 derivative.

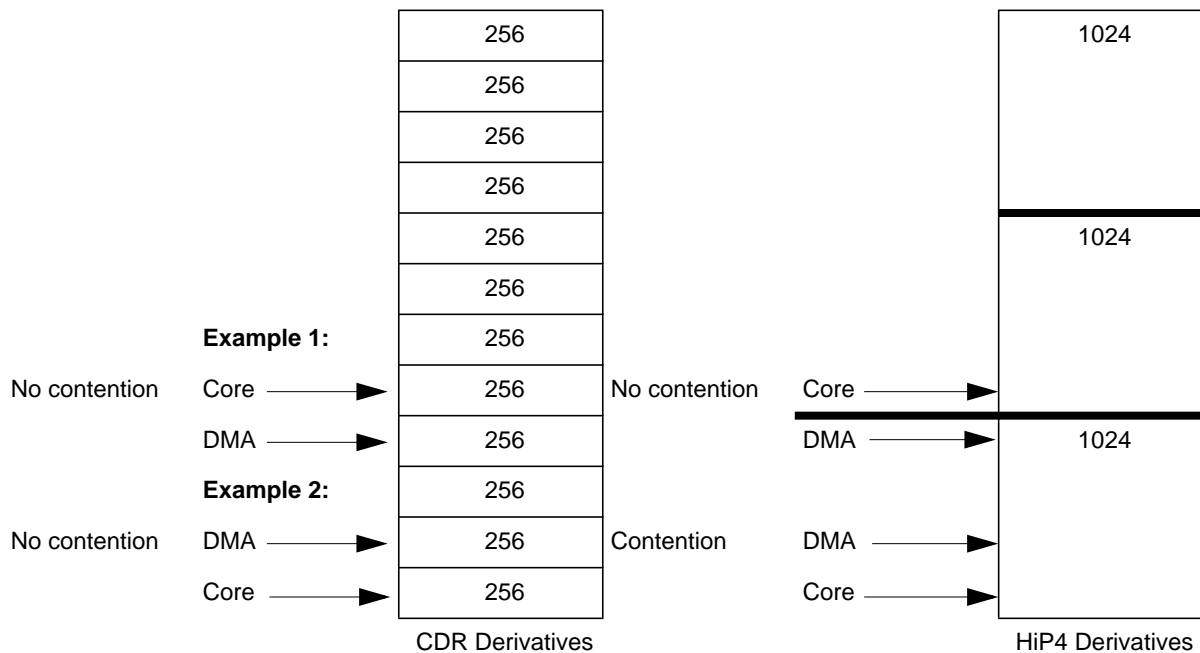


Figure C-1. CDR/HIP DMA and Core Access Comparisons

The same change in block size applies to EFCOP/core contention in derivatives that contain an EFCOP. Unlike Core/DMA contention, EFCOP/core contention may result in faulty data output in the Filter Data Output Register. For example, in the DSP56307, contention occurs if the EFCOP and core attempt to access the same 256 word block. In HiP4 derivatives, contention occurs if the EFCOP and core attempt to access the same 1 K word block. Both the DSP56307 and future HiP4 derivatives include the Data/Coefficient Transfer Contention (FCONT) bit in the EFCOP Control Status Register. The FCONT bit allows programmers to detect when EFCOP/core contention occurs.