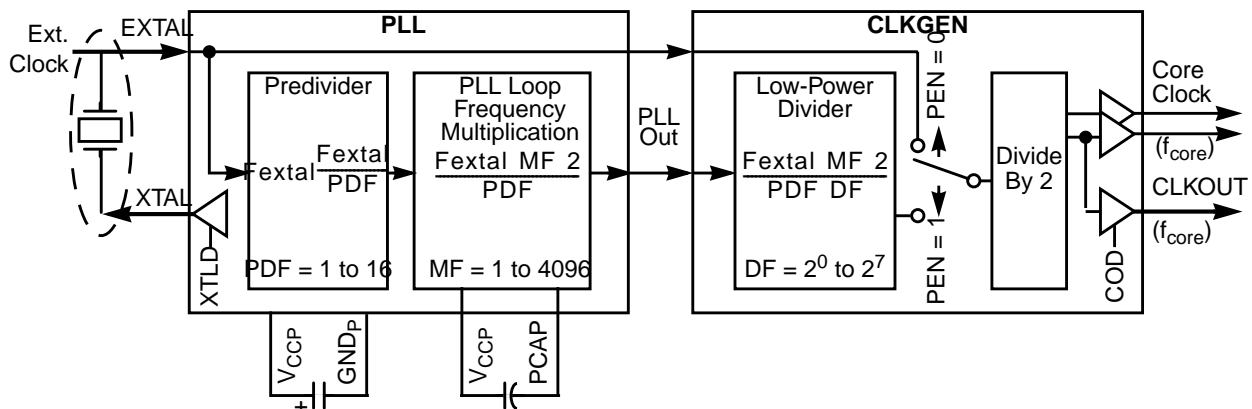


Chapter 6

PLL and Clock Generator

The DSP56300 core features a Phase Locked Loop (PLL) clock generator in its central processing module. The PLL allows the processor to operate at a high internal clock frequency derived from a low-frequency clock input, a feature that offers two immediate benefits. The lower frequency clock input reduces the overall electromagnetic interference generated by a system. The ability to oscillate at different frequencies reduces costs by eliminating the need to add additional oscillators to a system. **Figure 6-1** shows the two main blocks of the clock generator in the DSP56300 core:

- Phase Locked Loop (PLL) that performs:
 - Clock input division
 - Frequency multiplication
 - Skew elimination
- Clock Generator (CLKGEN) that performs:
 - Low-power division
 - Internal and external clock generation



Notes: The clock source can be either an external source applied to EXTAL, or a crystal connected to EXTAL and XTAL as a crystal oscillator configuration or connection.

Figure 6-1. PLL Clock Generator Block Diagram

6.1 PLL and Clock Signals

The PLL and clock pin configuration for each DSP56300 family member is available in the device-specific technical data sheet. The following pins are dedicated to the PLL and clock operation:

- **PCAP:** Connects an off-chip capacitor to the PLL filter. One terminal of the capacitor connects to PCAP, the other connects to V_{CCP} . The value of this capacitor depends on the PLL Multiplication Factor (MF). See the device-specific technical data sheet for the correct formula to use for this calculation.
- **CLKOUT:** Provides a 50 percent duty cycle output clock synchronized to the internal processor clock when the PLL is enabled and locked. When the PLL is disabled, the output clock at CLKOUT is derived from EXTAL, and has half the frequency of, EXTAL. This pin is operational in all device processing states except when the PLL Control 1(PCTL1) Register Clock Out Disable (COD) bit is set, and during the Stop state. When the device is in the Wait state, the CLKOUT pin continues to provide a signal.
- **PINIT:** During assertion of hardware reset, the value of the PINIT input pin is written into the PCTL1 PLL Enable (PEN) bit. After hardware reset is deasserted, the PLL ignores the PINIT pin, and it can have a different function in the device.
- **PLOCK:** Originates from the Phase Detector. The device asserts PLOCK when the PLL is enabled and locked. When the device deasserts PLOCK output, the PLL is enabled but not locked. PLOCK is also asserted when the PLL is disabled. PLOCK is a reliable indicator of the PLL lock state only after exiting the hardware reset state.

6.2 PLL Block

Figure 6-2 shows the PLL block diagram. This section describes the PLL control mechanisms.

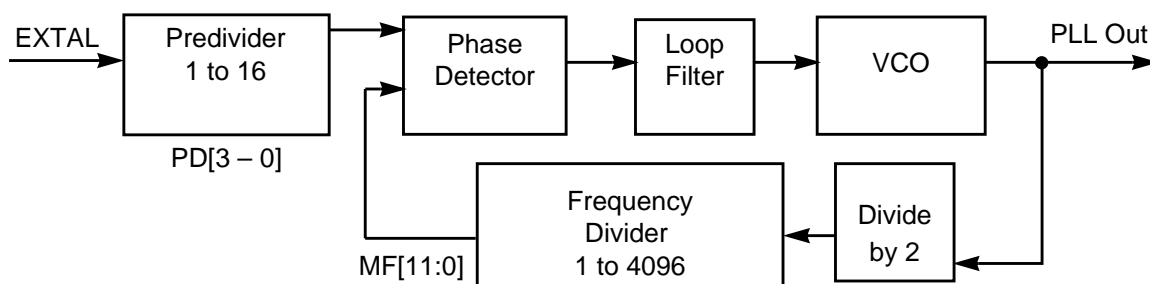


Figure 6-2. PLL Block Diagram

6.2.1 Frequency Predivider

Clock input frequency division is accomplished by means of a frequency predivider of the input frequency. The programmable Division Factor ranges from 1 to 16.

6.2.2 Phase Detector and Charge Pump Loop Filter

The Phase Detector (PD) detects any phase difference between the external clock (EXTAL) and the phase of the clock generated by the frequency divider. At the point where there is negligible phase difference and the frequency of the two inputs is identical, the PLL is in the Locked state. The charge pump loop filter receives signals from the PD and either increases or decreases the phase based on the PD signals. An external capacitor is connected to the PCAP input to determine low pass filter corner frequencies. The value of this capacitor depends on the Multiplication Factor (MF) of the PLL. See the Specifications section in the device-specific technical data sheet for the formula to determine the proper value for the PLL capacitor. After the PLL locks onto the proper phase and frequency, it reverts to the Narrow Bandwidth mode, which is useful for tracking small changes due to frequency drift of the EXTAL clock.

6.2.3 Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator (VCO) can oscillate at frequencies from the minimum speed up to the maximum allowed clock input frequency. See the device-specific technical data sheet for these speeds.

Note: When the PLL is enabled, the device operating frequency is half of the VCO oscillating frequency.

If EXTAL is less than the VCO minimum working frequency, the hardware design should hold the PINIT input low during hardware reset. Following reset, the software can change MF to the desired value, and set the PCTL[PEN] bit.

6.2.3.1 Divide by 2

The output of the VCO is divided by 2. This results in a constant $\times 2$ multiplication of the PLL clock output used to generate the special device clock phases.

6.2.3.2 Frequency Divider

The Frequency Divider, which connects to the feedback loop of the PLL, multiplies the incoming external clock. In the PLL closed loop, the effect of the frequency divider is to multiply the PLL input frequency by its Division Factor. Therefore, the terms “Frequency Multiplication” and “Frequency Division” are used interchangeably in this chapter. The programmable Division Factor ranges from 1 to 4096, resulting in frequency

multiplication in the same range. This factor is programmable using the PCTL MF[11 – 0] bits.

6.2.3.3 PLL Control Elements

The PLL uses three major control elements in its circuitry:

- Clock input division
- Frequency multiplication
- Skew elimination

6.2.3.3.1 Clock Input Division

The PLL can divide the input frequency by any integer between 1 and 16. The combination of input division and output low-power division enables you to generate almost every frequency value out of the PLL (see **Section 6.2.3.3.7**, "Operating Frequency," on page 6-6). The Division Factor can be modified by changing the value of the PCTL Predivider Factor (PDF) bits (PD[3 – 0]). The output frequency of the predivider is determined using the following formula:

$$\frac{F_{\text{EXTAL}}}{\text{PDF}}$$

6.2.3.3.2 Frequency Multiplication

The PLL can multiply the input frequency by any integer between 1 and 4096. The Multiplication Factor can be modified by changing the value of the PCTL Multiplication Factor (MF[11 – 0]) bits. The output frequency of the PLL (that is, PLL Out as shown in **Figure 6-1** on page 6-1) is computed using the following formula:

$$\frac{F_{\text{EXTAL}} \times \text{MF} \times 2}{\text{PDF}}$$

6.2.3.3.3 Skew Elimination

The phase skew of the PLL is defined as the time difference between the falling edges of EXTAL and CLKOUT for a given capacitive load on CLKOUT, over the entire process, temperature, and voltage ranges. The PLL can eliminate the skew between the external clock (EXTAL), the internal clock phases, and the CLKOUT signal, allowing tighter synchronous timings. Skew elimination is active only when the PLL is enabled and programmed with a Multiplication Factor less than or equal to 4. When the PLL is disabled, or when the Multiplication Factor is greater than 4, clock skew can exist.

Note: Skew elimination is assured only if EXTAL is greater than the minimum frequency specified in the device-specific technical data sheet (typically 15 MHz).

6.2.3.3.4 Clock Generator

Figure 6-3 on page 6-5 shows the Clock Generator block diagram. The components of the Clock Generator are described in the following sections.

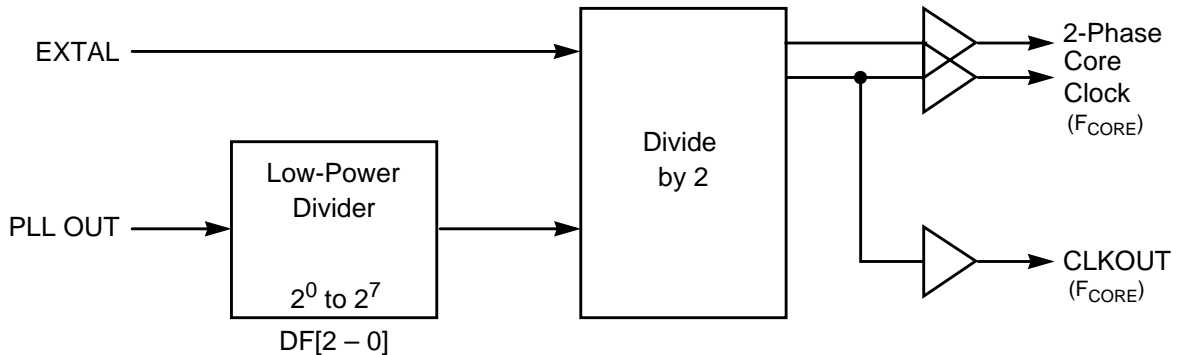


Figure 6-3. CLKGEN Block Diagram

6.2.3.3.5 Low-Power Divider (LPD)

The Clock Generator has a divider connected to the output of the PLL. The Low-Power Divider (LPD) divides the output frequency of the VCO by any power of 2 from 2^0 to 2^7 . The Division Factor (DF) of the LPD can be modified by changing the value of the PLL Control Register (PCTL) Division Factor bits DF[2 – 0]. Since the LPD is not in the closed loop of the PLL, changes in the DF do not cause a loss of lock condition. The result is a significant power savings when the LPD operates in low-power consumption modes as the device is not involved in intensive calculations. When the device is required to exit a low-power mode, it can immediately do so with no time needed for clock recovery or PLL lock.

6.2.3.3.6 Internal and External Clock Pulse Generator

The output stage of the Clock Generator generates the clock signals to the core and the device peripherals, and drives the CLKOUT pin. The output stage divides the frequency by two. The input source to the output stage is selected between:

- EXTAL (PEN = 0, PLL disabled), which generates a device frequency defined by the following formula:

$$\frac{F_{EXTAL}}{2}$$

- Low-Power Divider output (PEN = 1, PLL enabled), which generates a device frequency defined by the following formula:

$$\frac{F_{EXTAL} \times MF}{PDF \times DF}$$

6.2.3.3.7 Operating Frequency

When PEN = 1, the operating frequency of the core is governed by the frequency control bits in the PCTL Register according to the following formula:

$$F_{CORE} = \frac{F_{EXTAL} \times MF}{PDF \times DF}$$

where:

- MF is the Multiplication Factor defined by MF[11 – 0]
- PDF is the Predivider Factor defined by PD[3 – 0]
- DF is the Division Factor defined by DF[2 – 0]
- F_{CORE} is the device operating frequency
- F_{EXTAL} is the external EXTAL input

6.3 PLL Programming Model

The PLL clock generator uses a single register, the PCTL Register. The PCTL is an X I/O mapped 24-bit read/write register used to direct the operation of the on-chip PLL. **Figure 6-4** shows the PCTL control bits.

23	22	21	20	19	18	17	16	15	14	13	12
PD3	PD2	PD1	PD0	COD	PEN	PSTP	XTLD	XTLR	DF2	DF1	DF0
11	10	9	8	7	6	5	4	3	2	1	0
MF11	MF10	MF9	MF8	MF7	MF6	MF5	MF4	MF3	MF2	MF1	MF0

Figure 6-4. PLL Control Register (PCTL)

Table 6-1. PLL Control Register (PCTL) Bit Definitions

Bit Number	Bit Name	Reset Value	Description	
23 – 20	PD		<p>Predivider Factor Define the PDF value that is applied to the input frequency. PDF can be any integer from 1 to 16. The VCO oscillates at a frequency defined by the following formula:</p> $\frac{F_{\text{EXTAL}} \times \text{MF} \times 2}{\text{PDF}}$ <p>PDF must be chosen to ensure that the resulting VCO output frequency lies in the range specified in the device-specific technical data sheet. Any time a new value is written into the PD[3 – 0] bits, the PLL loses the lock condition. After a time delay (zero to 1,000 clock cycles), the PLL relocks. The PDF bits (PD[3 – 0]) are set to a predetermined value during hardware reset. The reset value is implementation dependent and is listed in the device-specific user's manual.</p>	
			PD[3 – 0]	PDF Value
			0000	1
			0001	2
			0010	3
			0011	4
			0100	5
			0101	6
			0110	7
			0111	8
			1000	9
			1001	10
			1010	11
			1011	12
			1100	13
			1101	14
1110	15			
1111	16			
19	COD	0	<p>Clock Output Disable Controls the output buffer of the clock at the CLKOUT pin. When COD is set, the CLKOUT output is pulled high. When COD is cleared, the CLKOUT pin provides a 50 percent duty cycle clock synchronized to the internal core clock. If CLKOUT is not connected to external circuits, set COD (disabling clock output) to minimize RFI noise and power dissipation. The CLKOUT pin oscillates during all operating states except Stop state and when COD = 1.</p>	

Table 6-1. PLL Control Register (PCTL) Bit Definitions (Continued)

Bit Number	Bit Name	Reset Value	Description																										
18	PEN		<p>PLL Enable Enables PLL operation. When PEN is set, the PLL is enabled and the internal clocks are derived from the PLL VCO output. When PEN is cleared, the PLL is disabled and the internal clocks are derived directly from the EXTAL signal. When the PLL is disabled, the VCO stops to minimize power consumption. The PEN bit may be set or cleared by software any time during the device operation. During hardware reset, this bit is set or cleared based on the value of the PLL PINIT input.</p>																										
17	PSTP	0	<p>PLL Stop State Controls PLL and on-chip crystal oscillator behavior during the Stop processing state. When PSTP is set, the PLL and the on-chip crystal oscillator remain operating when the chip is in the Stop state. When PSTP is cleared and the device enters the Stop state to support minimum power consumption, the PLL and the on-chip crystal oscillator are disabled, to further reduce power consumption; this however results in longer recovery time upon exit from the Stop state. To enable rapid recovery when exiting the Stop state (but at the cost of higher power consumption during the Stop state), PSTP should be set.</p> <p>NOTE: PSTP and PEN are related. When PSTP is set, and PEN is cleared, the on-chip crystal oscillator remains operating in the Stop state, but the PLL is disabled. This power saving feature enables rapid recovery from the Stop state when you operate the device with an on-chip oscillator and with the PLL disabled.</p> <table border="1"> <thead> <tr> <th rowspan="2">PSTP</th> <th rowspan="2">PEN</th> <th colspan="2">Operation During Stop State</th> <th rowspan="2">Recovery Time From Stop State</th> <th rowspan="2">Power Consumption During Stop State</th> </tr> <tr> <th>PLL</th> <th>Oscillator</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>x</td> <td>Disabled</td> <td>Disabled</td> <td>Long</td> <td>Minimal</td> </tr> <tr> <td>1</td> <td>0</td> <td>Disabled</td> <td>Enabled</td> <td>Short</td> <td>Lower</td> </tr> <tr> <td>1</td> <td>1</td> <td>Enabled</td> <td>Enabled</td> <td>Short</td> <td>Higher</td> </tr> </tbody> </table>	PSTP	PEN	Operation During Stop State		Recovery Time From Stop State	Power Consumption During Stop State	PLL	Oscillator	0	x	Disabled	Disabled	Long	Minimal	1	0	Disabled	Enabled	Short	Lower	1	1	Enabled	Enabled	Short	Higher
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0	x	Disabled	Disabled	Long	Minimal																								
1	0	Disabled	Enabled	Short	Lower																								
1	1	Enabled	Enabled	Short	Higher																								
16	XTLD		<p>XTAL Disable Controls the XTAL output from the crystal oscillator on-chip driver. When XTLD is cleared, the XTAL output pin is active, permitting normal operation of the crystal oscillator. When XTLD is set, the XTAL output pin is pulled high, disabling the on-chip oscillator driver. If the on-chip crystal oscillator driver is not used (that is, EXTAL is driven from an external clock source), set XTLD (disabling XTAL) to minimize RFI noise and power dissipation.</p> <p>NOTE: The XTLD bit is set to a predetermined value during hardware reset. The value is implementation dependent and may vary between different DSP56300-based devices.</p>																										

Table 6-1. PLL Control Register (PCTL) Bit Definitions (Continued)

Bit Number	Bit Name	Reset Value	Description																		
15	XTLR		<p>Crystal Range Controls the on-chip crystal oscillator transconductance. If the external crystal frequency is less than 200 kHz (that is, a 32 KHz clock crystal), set this bit to decrease the transconductance of the input amplifier. Otherwise, the internal clocks may not be stable. If the external crystal frequency is greater than 200 kHz, clear this bit in order to have full transconductance. Otherwise, the crystal oscillator may not function at all.</p> <p>NOTE: The XTLR bit is set to a predetermined value during hardware reset. The value is implementation dependent and may vary between different DSP56300-based devices.</p>																		
14 – 12	DF	0	<p>Division Factor Define the DF of the low-power divider. These bits specify the DF as a power of two in the range from 2^0 to 2^7. Changing the value of the DF[2 – 0] bits does not cause a loss of lock condition. Whenever possible, changes of the operating frequency of the device (for example, to enter a low-power mode) should be made by changing the value of the DF[2 – 0] bits rather than changing the MF[11 – 0] bits.</p> <p>For $MF \leq 4$, changing DF[2 – 0] may lengthen the instruction cycle following the PLL control register update; this ensures synchronization between EXTAL and the internal device clock. For $MF > 4$ such synchronization is not ensured, and the instruction cycle is not lengthened.</p> <table border="1"> <thead> <tr> <th>DF[2 – 0]</th> <th>DF Value</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>2^0</td> </tr> <tr> <td>001</td> <td>2^1</td> </tr> <tr> <td>010</td> <td>2^2</td> </tr> <tr> <td>011</td> <td>2^3</td> </tr> <tr> <td>100</td> <td>2^4</td> </tr> <tr> <td>101</td> <td>2^5</td> </tr> <tr> <td>110</td> <td>2^6</td> </tr> <tr> <td>111</td> <td>2^7</td> </tr> </tbody> </table>	DF[2 – 0]	DF Value	000	2^0	001	2^1	010	2^2	011	2^3	100	2^4	101	2^5	110	2^6	111	2^7
DF[2 – 0]	DF Value																				
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100	2^4																				
101	2^5																				
110	2^6																				
111	2^7																				

Table 6-1. PLL Control Register (PCTL) Bit Definitions (Continued)

Bit Number	Bit Name	Reset Value	Description														
11 – 0	MF		<p>Multiplication Factor Defines the Multiplication Factor (MF) that is applied to the PLL input frequency. The MF can be any integer from 1 to 4096. The VCO oscillates at a frequency defined by the following formula where PDF is the Predivider Division Factor:</p> $F_{\text{EXTAL}} \times \text{MF} \times \frac{2}{\text{PDF}}$ <p>The MF must be chosen to ensure that the resulting VCO output frequency is in the range specified in the device-specific technical data sheet. Any time a new value is written into the MF[11 – 0] bits, the PLL loses the lock condition. After a time delay (provided in the device-specific technical data sheet), the PLL relocks. The Multiplication Factor bits MF[11 – 0] are set to a predetermined value during hardware reset; the value is implementation dependent and is provided in the device-specific user's manual.</p> <table border="1"> <thead> <tr> <th>MF[11 – 0]</th> <th>Multiplication Factor MF</th> </tr> </thead> <tbody> <tr> <td>\$000</td> <td>1</td> </tr> <tr> <td>\$001</td> <td>2</td> </tr> <tr> <td>\$002</td> <td>3</td> </tr> <tr> <td>• • •</td> <td>• • •</td> </tr> <tr> <td>\$FFE</td> <td>4095</td> </tr> <tr> <td>\$FFF</td> <td>4096</td> </tr> </tbody> </table>	MF[11 – 0]	Multiplication Factor MF	\$000	1	\$001	2	\$002	3	• • •	• • •	\$FFE	4095	\$FFF	4096
MF[11 – 0]	Multiplication Factor MF																
\$000	1																
\$001	2																
\$002	3																
• • •	• • •																
\$FFE	4095																
\$FFF	4096																

6.4 Clock Synchronization

When the PLL is enabled, (the PEN bit in the PCTL register is set), low clock skew between EXTAL and CLKOUT is guaranteed if $\text{MF} < 5$. CLKOUT and the internal device clock are fully synchronized. See the device-specific technical data sheet for additional information.

6.5 Design Guidelines for Ripple and PCAP

The voltage noise on the VCCP pin is critical to the PLL operation, since the PLL loop filter capacitor connects to it. The following recommendations for filtering the PLL power supply apply to all DSP56300 family devices.

- The PLL power supply should be very well regulated and noise-free. Here are some recommendations for a V_{cc} noise filter for the PLL power supply:
 - The W_n (bandwidth) of the PLL is $2\text{MHz}/(\text{Multiplication Factor})$. The cutoff frequency of the V_{cc} filter should be less than $W_n/100$.
 - The maximum allowed accumulated noise at frequencies from $W_n/10$ to infinity is 6mV . The maximum allowed accumulated noise at frequencies from 0 Hz to $W_n/10$ is 30mV .
 - The filter should have as low as possible impedance for DC, in order to minimize voltage drop to the PLL power supplies.
 - Take care to ensure that no more than 0.5V voltage differential exists between the PLL power supply and the DSP power supplies at all times.

In the PLL filter circuit in **Figure 6-5**:

- Note that the 0.1F capacitor should be in parallel with the $22\mu\text{F}$, since the high frequency current needs for the PLL cannot be met with a regular $22\mu\text{F}$. If high-frequency noise is not attenuated due to the lack of this capacitor, it will come through the PCAP and cause jitter on the VCO. Beside that, the 12Ω with $22\mu\text{F}$ gives $F_c = 1/(2*3.14*12*22\text{u}) \sim 600\text{Hz}$,
- $W_n = 2\text{MHz} / 8 = 125\text{kHz}$, so the noise attenuation is expected to be about 50dB near DC, meaning that up to about 1Vp-p high-frequency noise may occur before the filter. For 4mA current consumption of the PLL, it means $V_{\text{drop}} = 12 * 4\text{mA} \approx 50\text{mV}$, which is also acceptable.

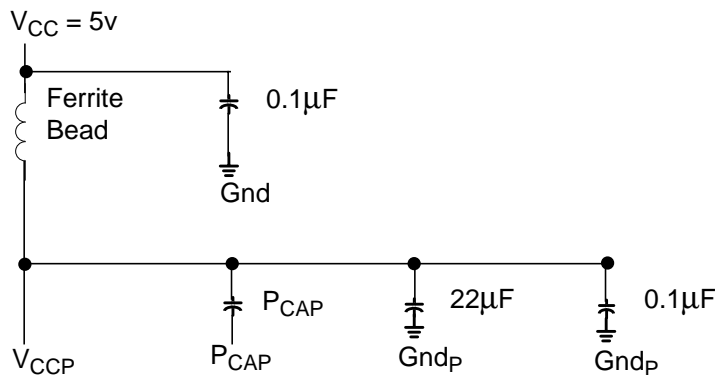


Figure 6-5. PLL Filter Circuit

NOTES:

1. FB = Ferrite Bead with 600Ω impedance at 100 MHz , 12Ω at DC.
2. PCAP value calculated according to datasheet.

