

In this problem the op-amps can be considered ideal except that the op-amp output voltage cannot exceed the limits equal to the supply voltages, $V_{omax} = V_{DD} = 5V$, $V_{omin} = -V_{SS} = -5V$. Switches have very small on-resistances R_{on} .

- a) Fig. (a) shows a switched-capacitor integrator. Find approximate $H(s) = v_o/v_i$ assuming that the signal frequencies are much smaller than the clock frequency f_s , i.e., using equivalent resistance. Is this SC integrator parasitic-insensitive? Justify your answer.

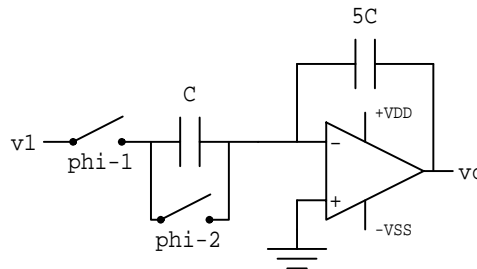


Fig.(a)

- b) Figure (b) shows a switched-capacitor voltage comparator that outputs a high level if $v_i < 0$ and a low level if $v_i > 0$. $V_B = V_{DD}/2$ is a constant dc voltage source. What are the high and the low voltage levels at the comparator output v_1 ?

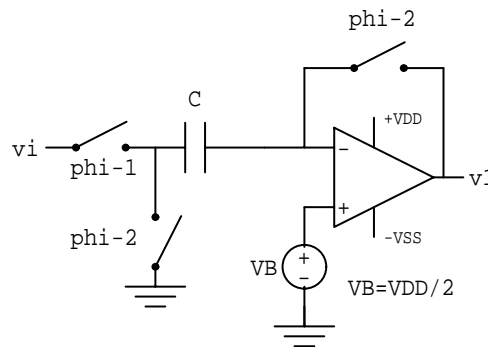


Fig.(b)

- c) Figure (c) shows timing diagrams of $v_i(t)$ in the comparator of Fig. (b), and the clocks ϕ_1, ϕ_2 . Sketch and label $v_1(t)$ in Fig. (c).
- d) The output $v_1(t)$ of the voltage comparator in Fig. (b) is connected to the input of the SC integrator in Fig. (a). Sketch and label the integrator output $v_o(t)$ in Fig. (c), assuming that the integrator output starts from 0 volts at $t = 0$. Would your result change if $V_B = 0$ instead of $V_{DD}/2$?

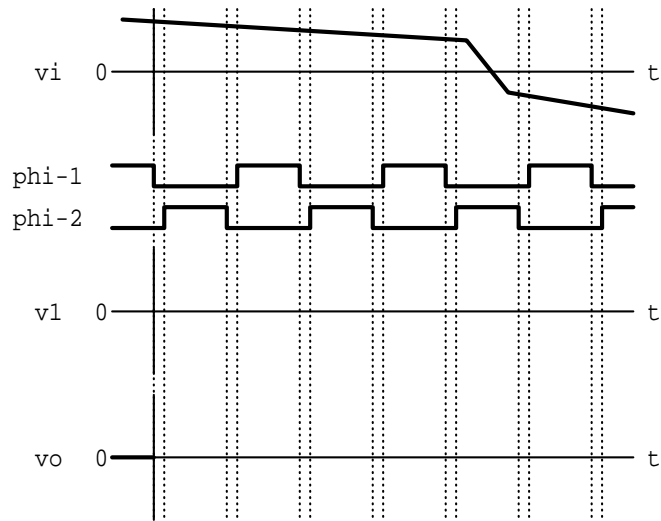


Fig.(c)