

Figure below shows a collection of switched-capacitor circuits. In all cases, assume that the switches have very low on resistance  $R_{on}$ , and that the op-amps are ideal except that the op-amp output voltage cannot exceed the limits equal to the supply voltages,  $V_{omax} = V_{DD} = 5\text{V}$ ,  $V_{omin} = -V_{SS} = -5\text{V}$ . All op-amps have the same supply voltages. Switch labels 1 and 2 stand for the non-overlapping clocks  $\phi_1, \phi_2$ . The sampling instants  $t = nT$  are at the high-to-low transitions of the  $\phi_1$  clock.

1. For the SC integrator in Fig. (a), find the transfer function  $H(z) = v_o/v_i$ , and the approximate  $H(s)$  assuming that the signal frequencies are much lower than the clock frequency  $f_s = 1/T$ .
2. Assuming  $v_i(t) = 0$  for  $t < 0$ ,  $v_i(t) = V_{DD} = 5\text{V}$ , for  $t \geq 0$ , and  $v_o(0) = 0$ , sketch the clock waveforms and  $v_o(t)$  for  $t \geq 0$ , for as long as  $v(t)$  changes in time. A high-to-low transition of  $\phi_2$  occurs at  $t = 0$ .
3. For the SC amplifier in Fig. (b), find the transfer function  $H(z) = v_o/v_i$ , and the approximate  $H(s)$  assuming that the signal frequencies are much lower than the clock frequency  $f_s$ .
4. For the SC voltage comparator in Fig. (c), find, sketch and label the input-to-output characteristic  $v_o(nT)$  as a function of  $v_i(nT)$ .
5. Fig. (d) shows how the SC circuits (a-c) are combined to construct an SC oscillator. All waveforms in Fig. (d) are periodic with the period equal to  $m/f_s$ . Assuming that a high-to-low transition of  $\phi_1$  occurs at  $t = 0$ , that  $v_{o1}(0) = 0$  and  $v_{o2}(0) = V_{DD}$ , sketch the clock waveforms and  $v_{o1}(t)$ ,  $v_{o2}(t)$  and  $v_{o3}(t)$  during one oscillation period. Find  $m$ .
6. Is it possible to reduce the number of switches in the oscillator of Fig. (d) without affecting the waveforms you found in part 5? If it is, sketch the circuit with the reduced number of switches.

