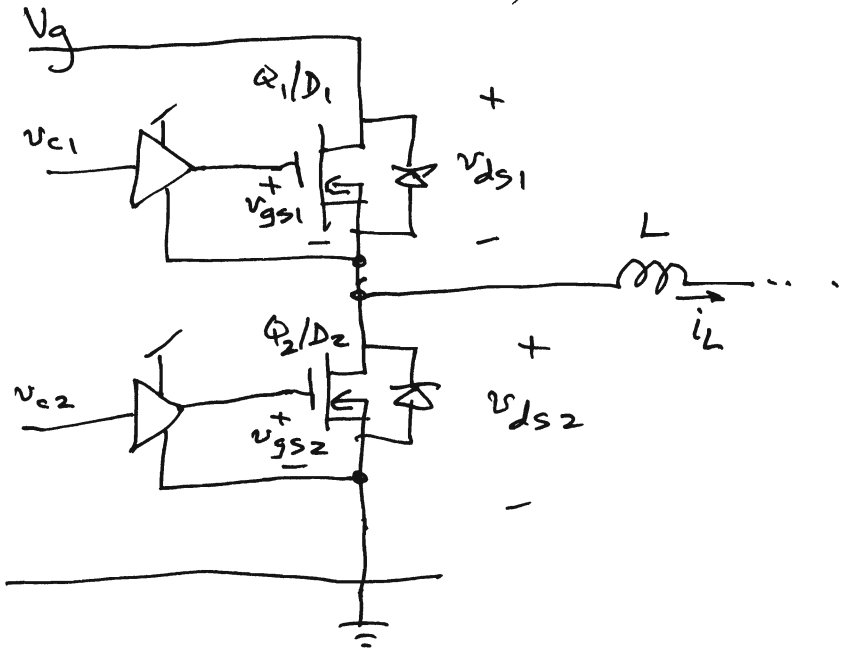
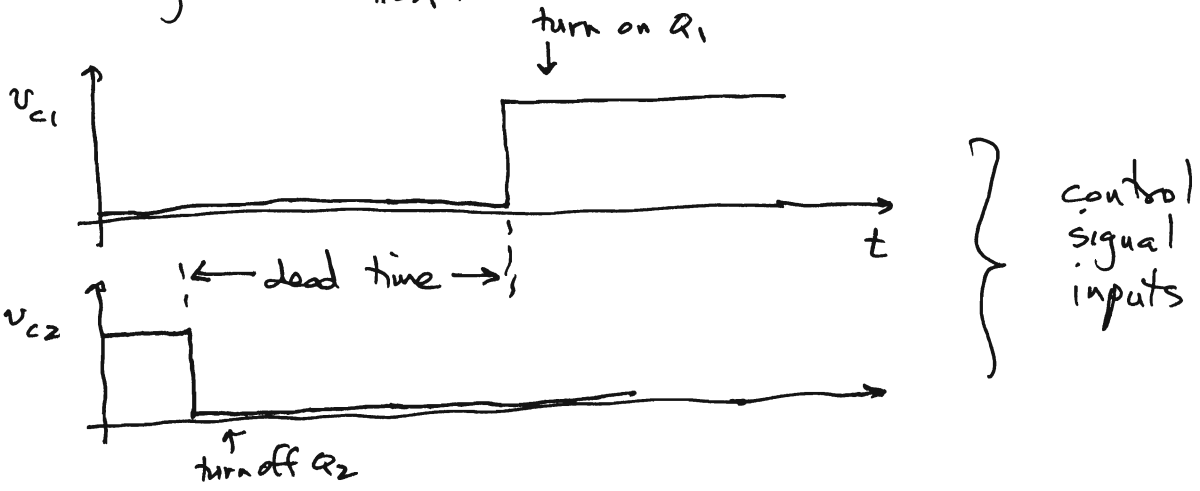
Driving synchronous switches

Avoiding "shoot through" current spikes caused by "cross-conduction" (simultaneous conduction) of synchronously switching MOSFETs



Let's assume $i_L > 0$, and examine the $Q_2 \rightarrow Q_1$ switching transition.

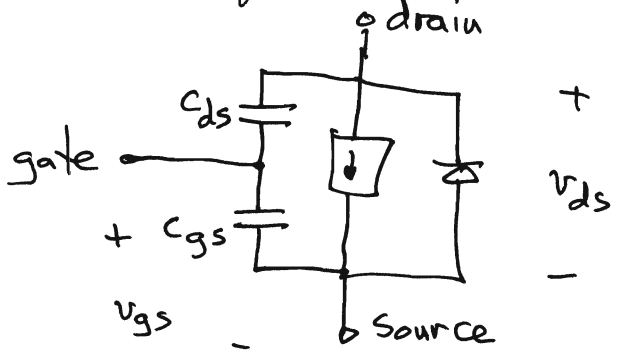


Dead time is inserted between the Q_2 turn off command and the Q_1 turn on command, to ensure that Q_1 and Q_2 do not simultaneously conduct. Typical dead times range from tens to hundreds of nanoseconds. The dead time is chosen to exceed the

worst-case difference between the driver turn-off and turn-on propagation delay times, plus the worst-case difference between the MOSFET turn-off and turn-on switching delay times.

Insertion of sufficient dead time is a good start, but it does not alone guarantee the absence of cross-conduction of Q_1 and Q_2. Even after the driver has turned off Q_2, it is possible for excessive $\frac{dv_{ds2}}{dt}$ to turn Q_2 on again. This can happen during the turn-on transition of Q_1.

MOSFET equivalent circuit

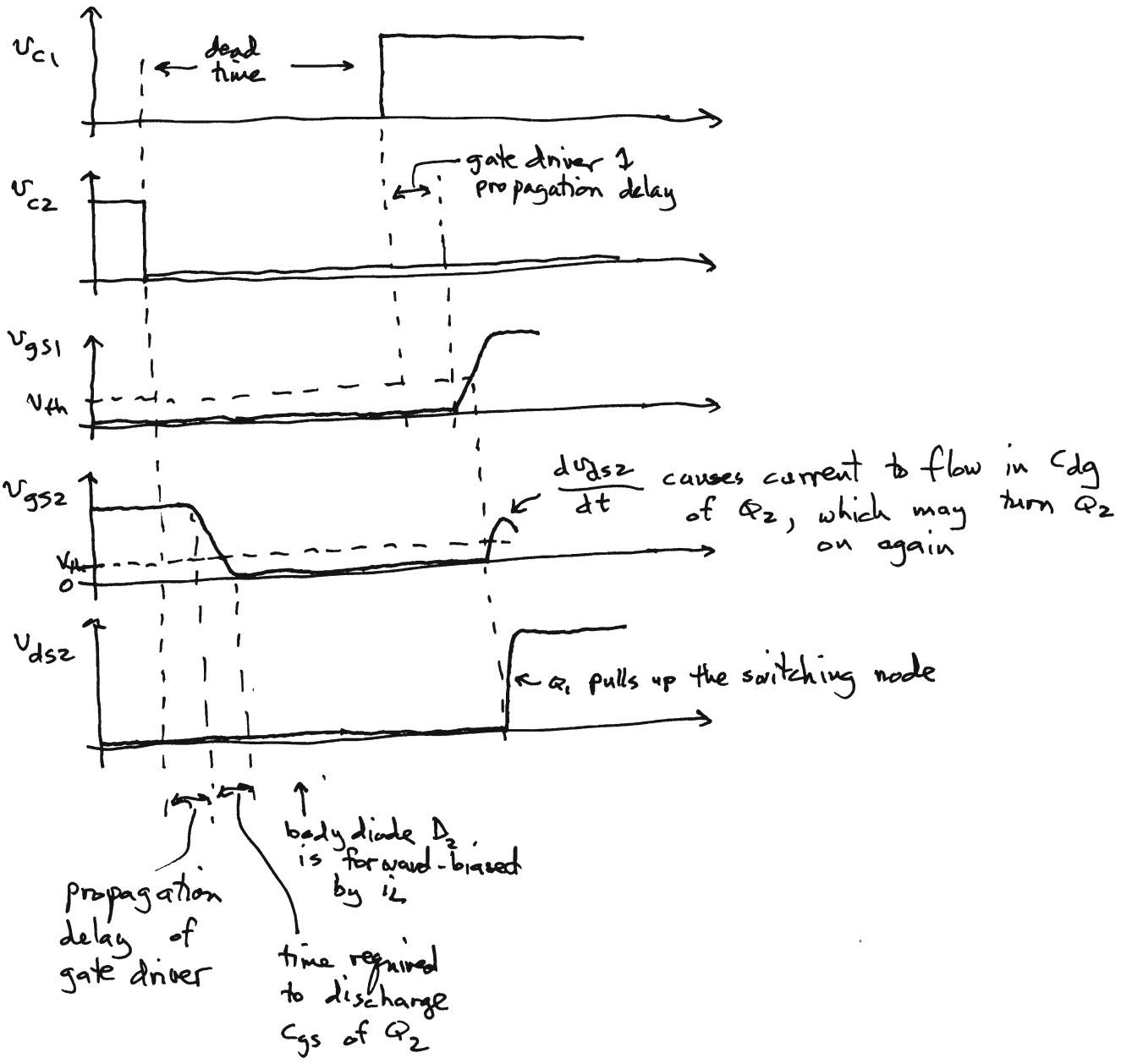


Although C_{ds} is substantially smaller than C_{gs}, the charge on C_{ds} can be large because of the large value of v_{ds}. Indeed, it is not unusual for Q_{gd} to exceed Q_{gs}.

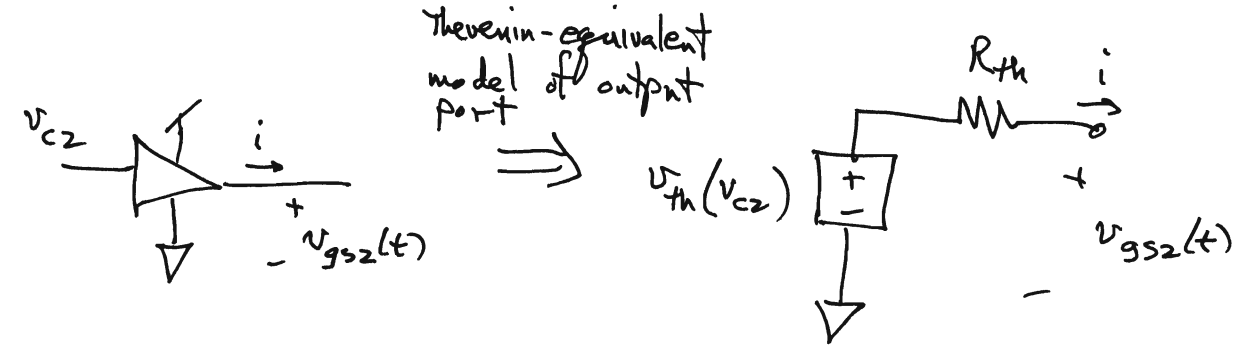
When v_{ds} changes, current flows through C_{ds}. This current can flow either through C_{gs} (thereby changing v_{gs}) or through the gate driver.

How well is the gate driver able to maintain $v_{gs}(t)$ at a constant desired value while C_{dg} charges?

In particular, can the gate driver keep Q_2 off by maintaining $v_{gs2}(t) < V_{th}$, during the turn-on transition of Q_1?



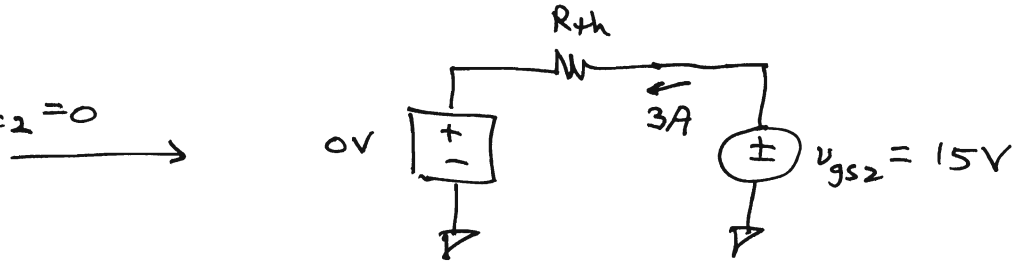
Gate driver equivalent circuit



Although the circuitry inside the gate driver is nonlinear, a linearized Thevenin equivalent model of the driver output port is reasonably accurate and gives insight into the problem considered here. The Thevenin resistance R_{th} depends on the size of the driver output-stage transistors, and possibly other quantities as well.

Datasheet specifications of the driver peak current capability amount to a specification of R_{th}. For example, a "3A gate driver" may be defined as follows:

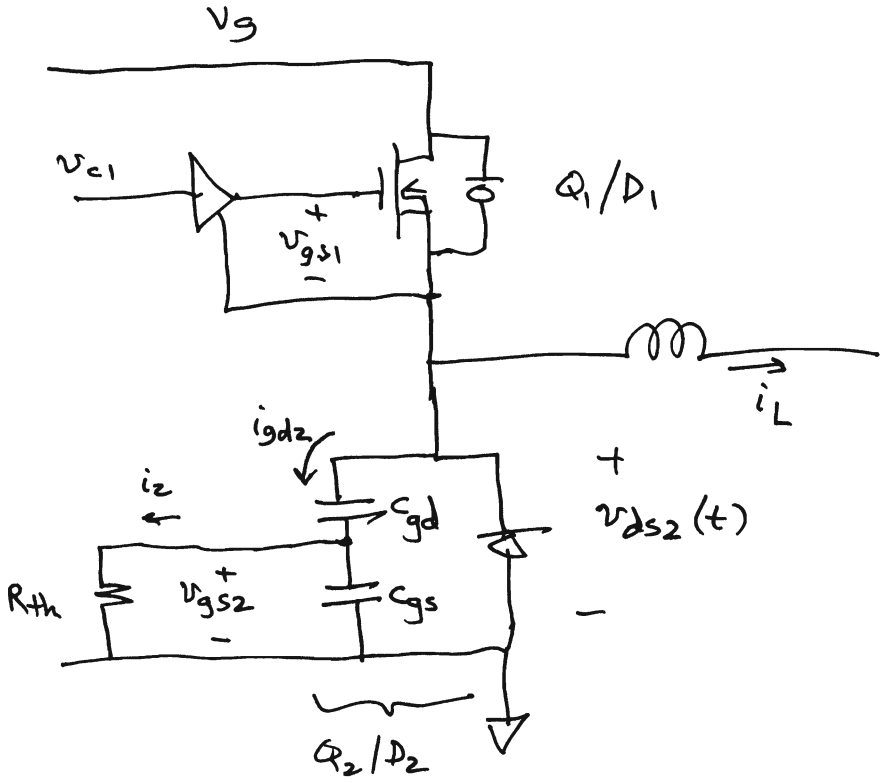
$i = -3A$ under the conditions $v_{c2} = 0$ and $v_{gs2} = 15V$



so $R_{th} = \frac{15V}{3A}$

$= 5\Omega$

So during the turn-on transition of Q_1, the Q_2 gate driver behaves as resistor R_{th} and the circuit is

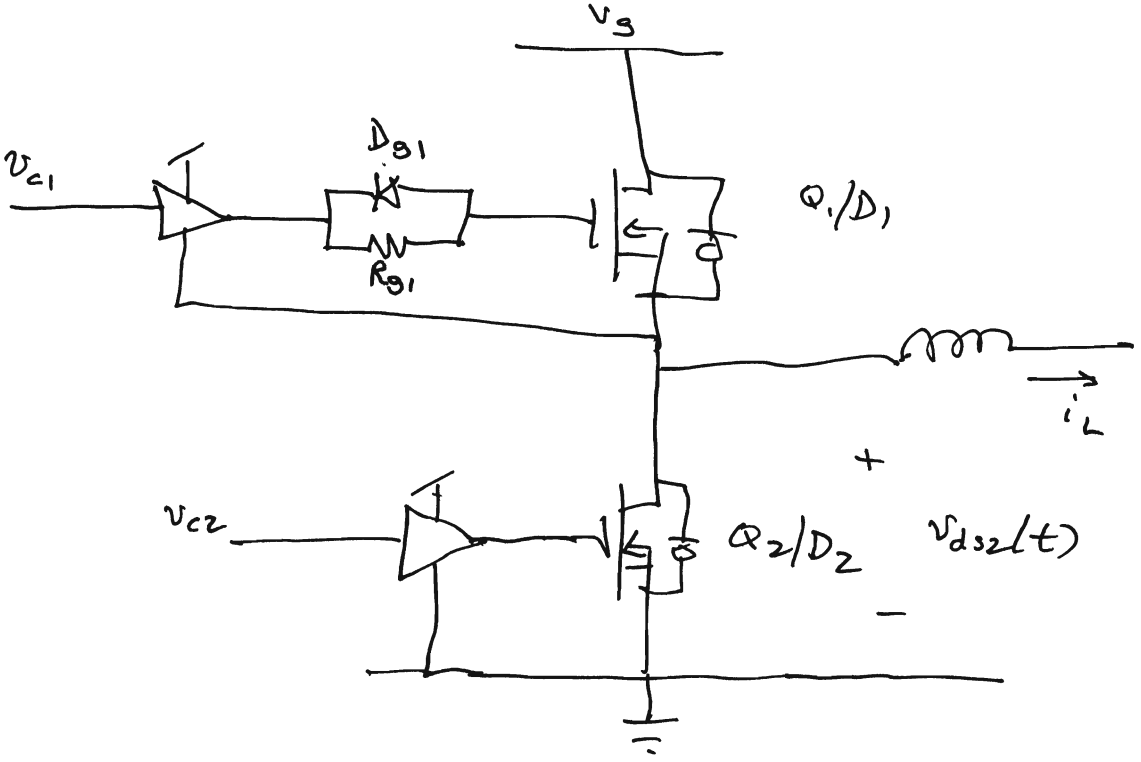


As long as v_{gs2} is zero, the driver current is $i_2 = \frac{v_{gs2}}{R_{th}} = 0$. So all of i_{gd2} flows (initially) into C_{gs} and causes v_{gs2} to increase.

Increasing v_{gs2} allows the driver to sink current $i_2 = \frac{v_{gs2}}{R_{th}}$. Is this sufficient to maintain $v_{gs2}(t) < V_{th}$ so that Q_2 remains off? It depends on the magnitude of $i_{gd2}(t)$, and hence on $\frac{dv_{ds2}(t)}{dt}$.

In practice, it is very easy for $\frac{dv_{ds2}}{dt}$ to turn Q_2 on again. When this happens, substantial oscillations in $v_{gs2}(t)$ and $v_{ds2}(t)$ are observed, and the switching loss is much greater than expected.

A common solution to this problem is the addition of a resistor/diode network that slows down the turn-on transition of Q_1:



R_{g1} is typically a few ohms or a few tens of ohms, and slows down the turn-on transition of Q_1. This reduces $dv_{ds2}(t)/dt$ sufficiently so that the Q_2 gate driver is able to hold Q_2 off during the

Q_1 turn-on transition. Diode D_{g1} allows Q_1 to be turned off quickly.

The above discussion applies to MOSFETS that operate as synchronous rectifiers. If i_L can reverse polarity, then an R_{g2}/D_{g2} network placed in series with the gate of Q_2 will protect the above phenomena from occuring in Q_1.

A small number of commercial gate drivers apply a negative voltage when the transistor is off. This achieves additional immunity from the $\frac{dv_{ds}}{dt}$ induced parasitic switching described above.