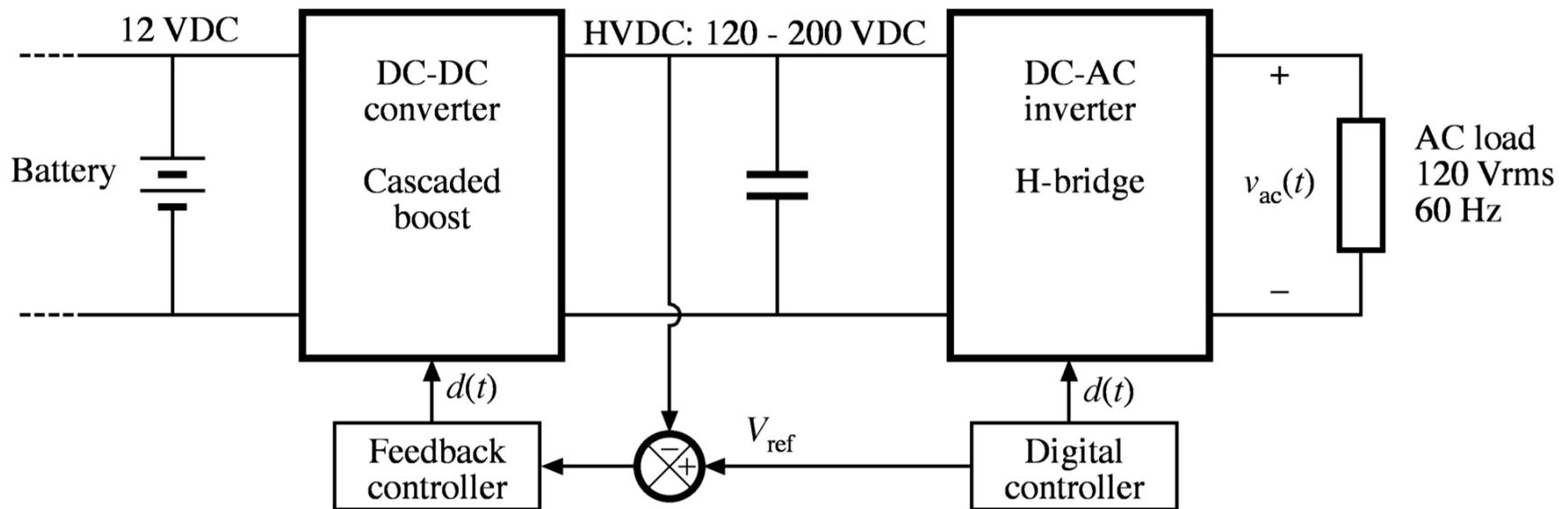


Lecture 7

ECEN 4517/5517

Experiments 4-5: inverter system



Exp. 4: *Step-up dc-dc converter (cascaded boost converters)*

Analog PWM and feedback controller to regulate HVDC

Exp. 5: *DC-AC inverter (H-bridge)*

Due dates

Now:

Quiz on Exp. 3 part 1.

This week in lab (Mar. 6 – 9):

Finish Exp. 3: get MPPT working outside.

Next week: noon on Tuesday Mar. 13

Prelab assignment for Exp. 4 (one from every student)

Next week: 5 pm on Friday Mar. 16:

Exp. 3 Part 2 final report (one per group)

Goals in upcoming weeks

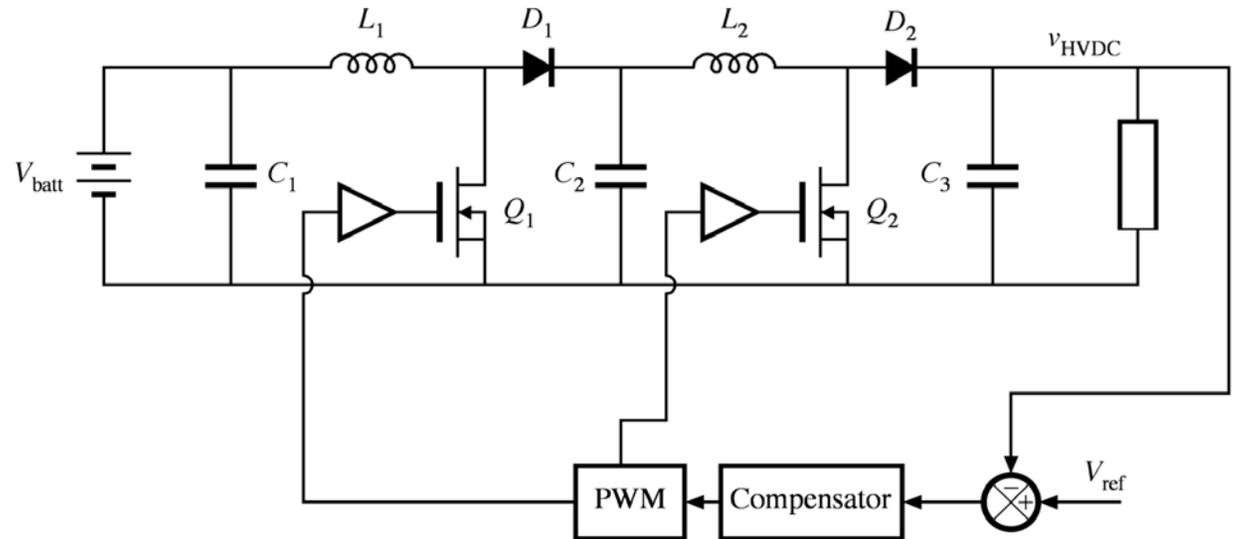
Exp. 4: Step-up dc-dc converter

Controller IC:

Demonstrate operating
PWM controller IC
(UC 3525)

Power Stage:

Demonstrate operating
power converter
(cascaded boost
converters)



Closed-Loop Analog Control System:

Demonstrate analog feedback system that regulates the dc output voltage
Measure and document loop gain and compensator design

Graduate Section:

Develop and verify system loss budget
Analytical model of control-to-output transfer function

Step-up DC-DC cascaded boost converters

Next week's prelab assignment

Need to step up the 12 V battery voltage to HVDC (120-200 V)

We will build inverter capable of producing same rated power as PV panel (85 W)

How much power can you get using the parts in your kit?

How efficient can your design be?

Key limitations:

- MOSFET on-resistances, rated voltages

- Capacitor rms current ratings, rated working voltages

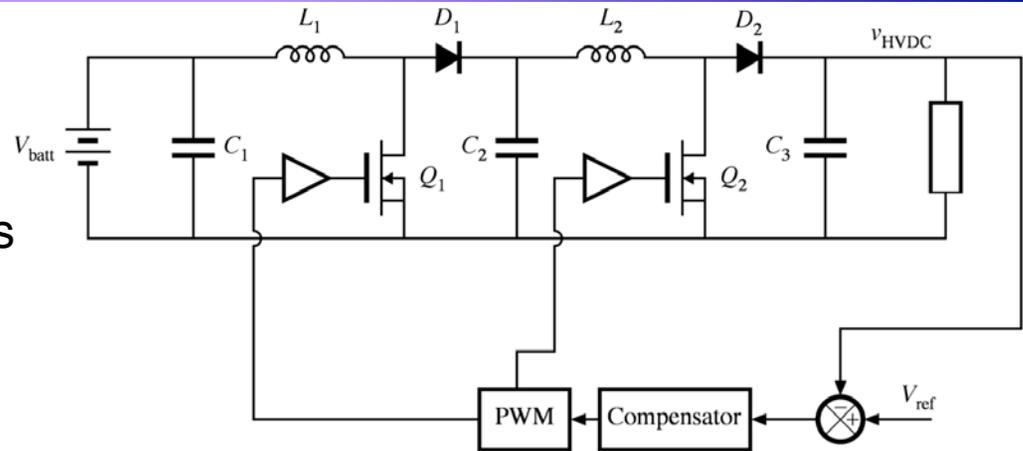
- Switching loss

- Inductor (core + dc copper + proximity) loss, saturation current

Need to choose duty cycles, switching frequency, inductances

Must ensure that all components operate within their specified limits

Design inductors



Converter loss budget

An example

Operating point: $V_{in} = 13 \text{ V}$, $V_{out} = 200 \text{ V}$, $P_{out} = 85 \text{ W}$

| | |
|--|--------------|
| MOSFET conduction loss | 2.2 W |
| Diode conduction loss | 1.5 W |
| Switching loss | 3.5 W |
| Inductor loss (core + dc copper + proximity) | <u>4.3 W</u> |
| Total loss: | 11.5 W |
| Predicted efficiency: | 88% |

(must document calculations to support above values)

The UC3525 PWM Control IC

Key functions:

Oscillator (sawtooth wave generator)

PWM comparator and latch

Error amplifier

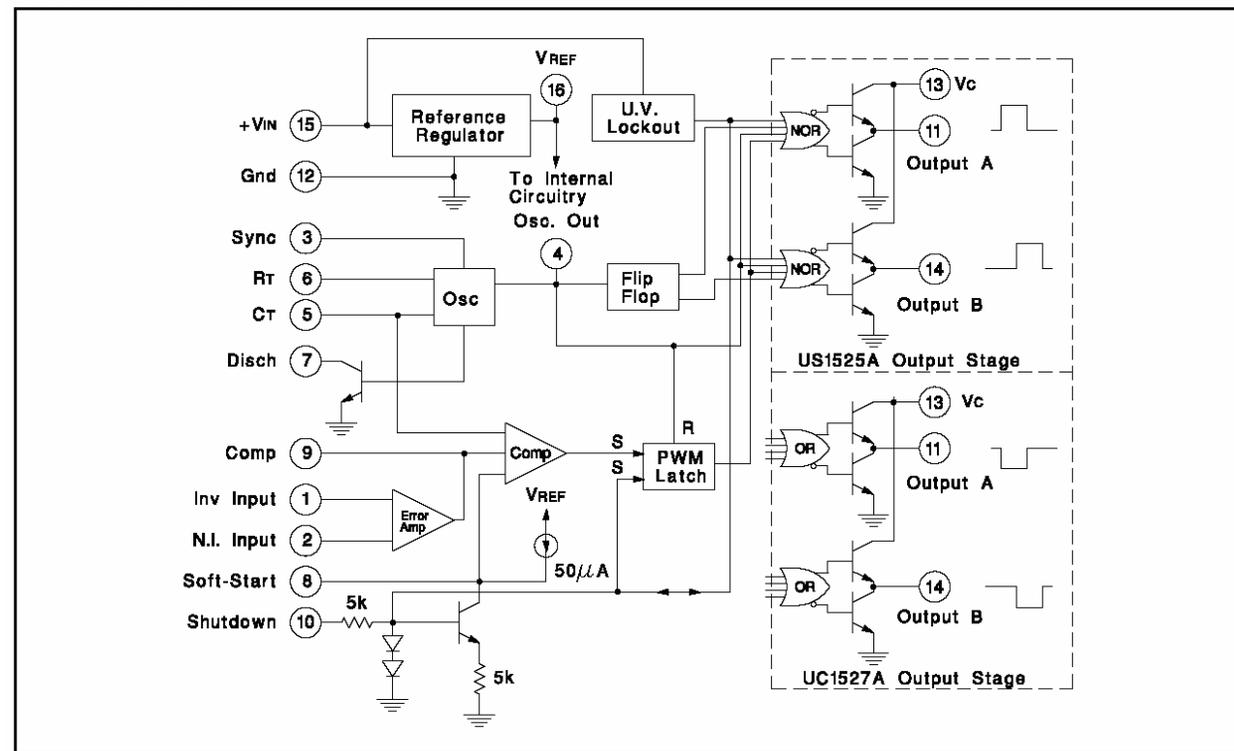
5.1 V reference

Pulse-steering logic

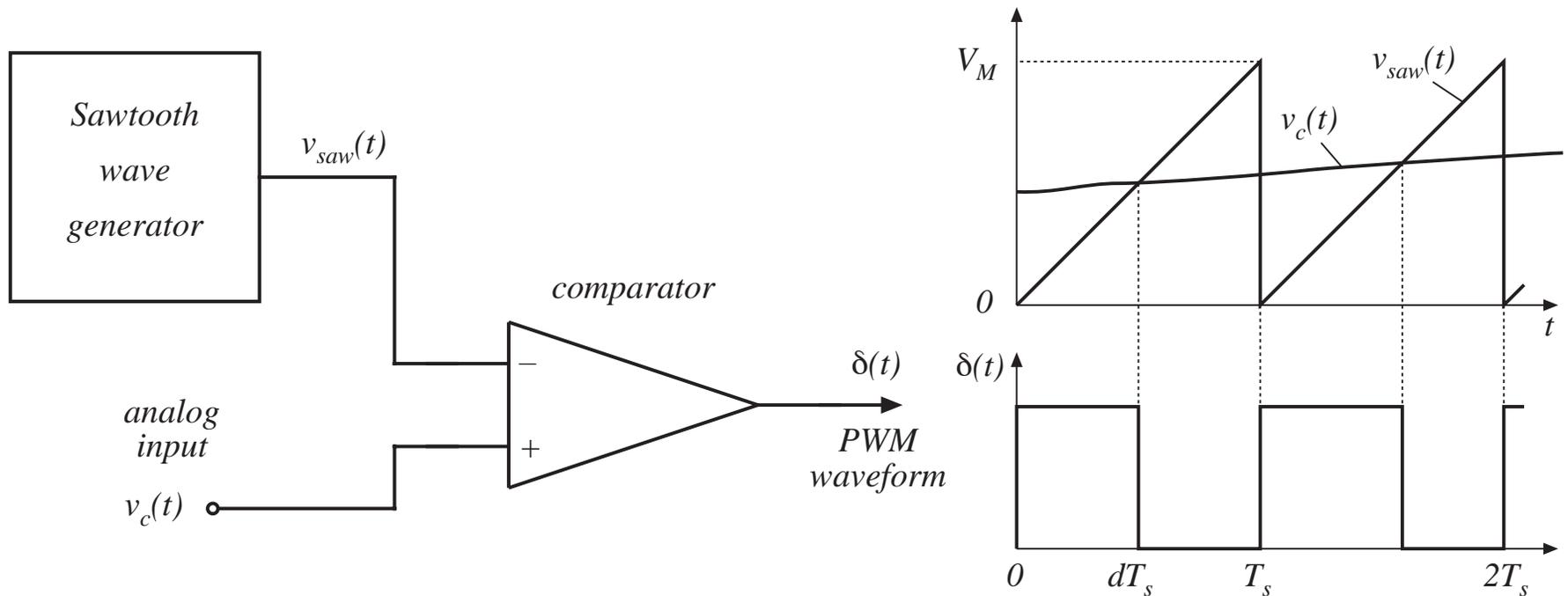
Output drivers

Shutdown and soft-start circuitry

BLOCK DIAGRAM



How a pulse-width modulator works

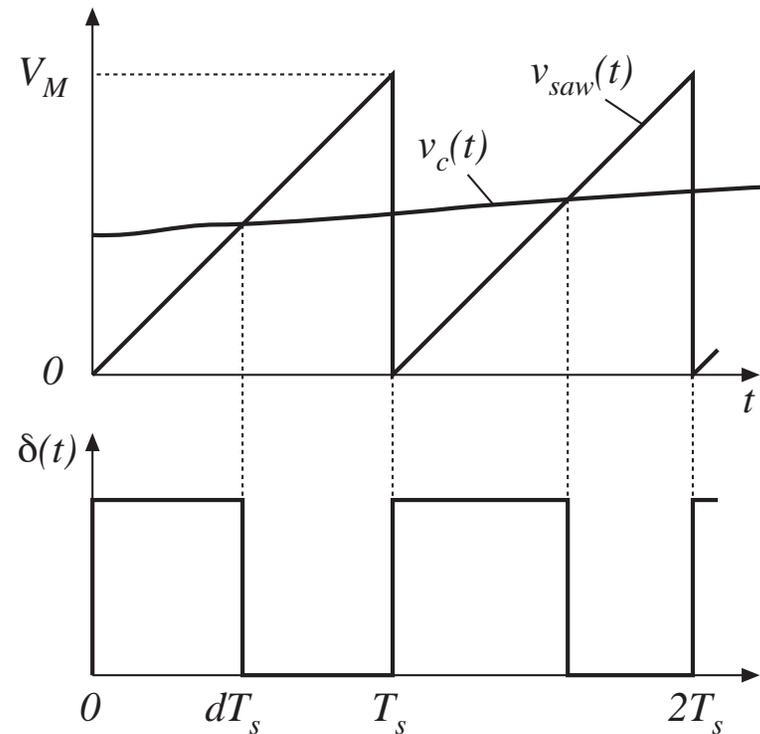


Equation of pulse-width modulator

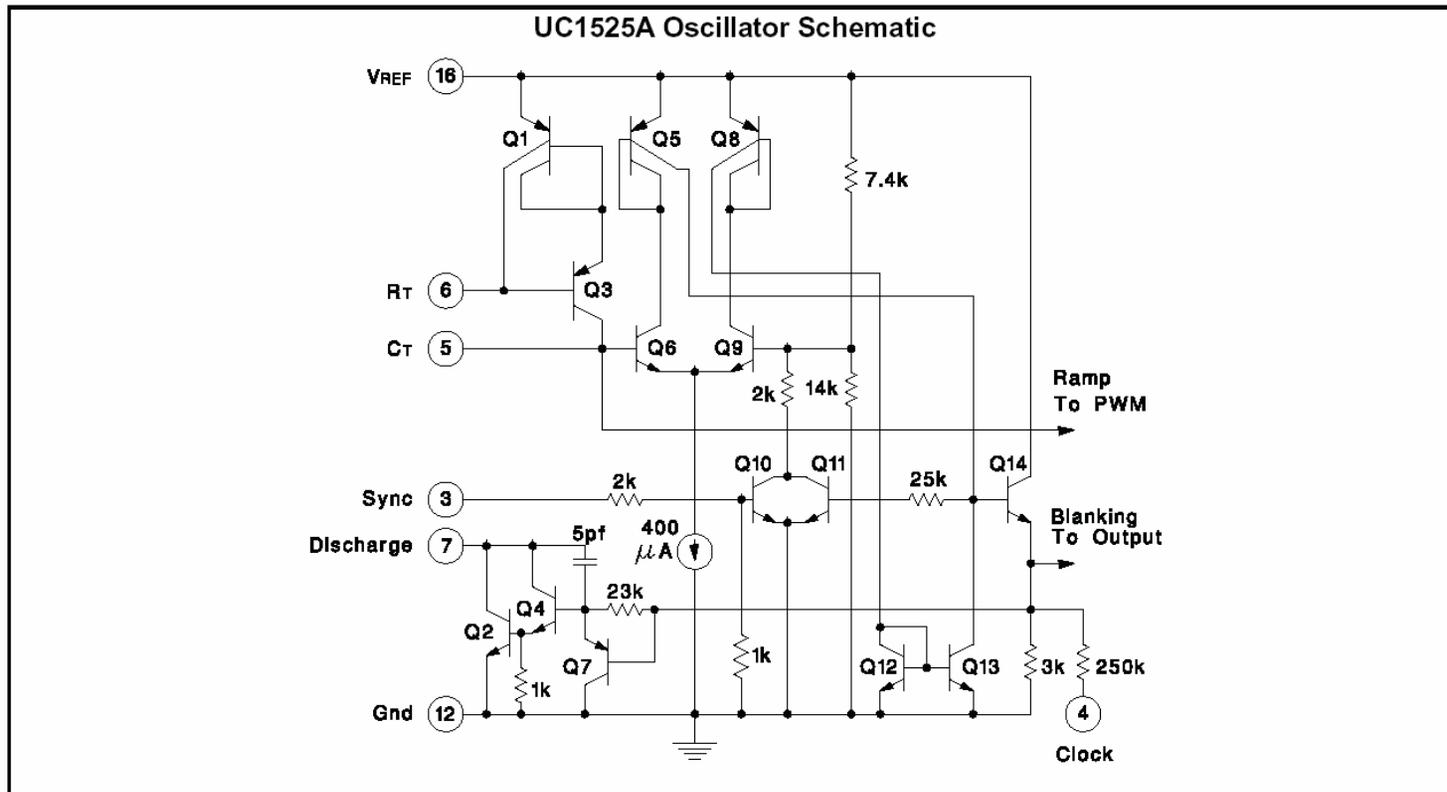
For a linear sawtooth waveform:

$$d(t) = \frac{v_c(t)}{V_M} \quad \text{for } 0 \leq v_c(t) \leq V_M$$

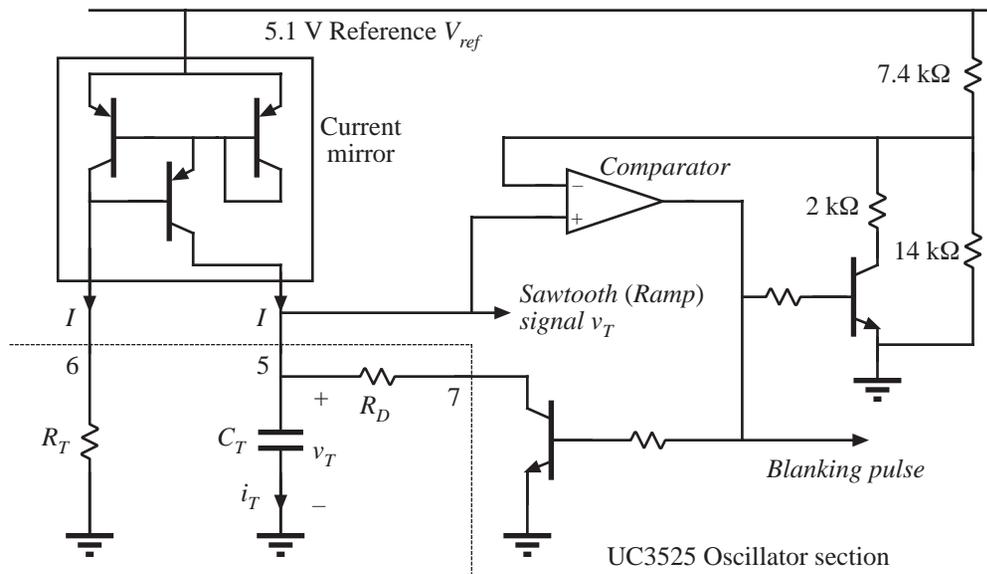
So $d(t)$ is a linear function of $v_c(t)$.



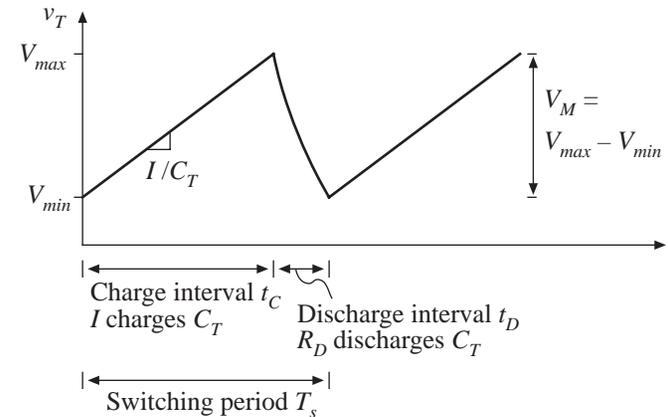
Sawtooth (Ramp) Oscillator



Simplified Block Diagram of Oscillator



$$i_T = C_T \frac{dv_T}{dt} \quad \text{hence} \quad \frac{dv_T}{dt} = \frac{i_T}{C_T}$$



$$I = \frac{(5.1 \text{ V}) - 2(0.7 \text{ V})}{R_T}$$

$$V_{\max} = (5.1 \text{ V}) \frac{14 \text{ k}\Omega}{14 \text{ k}\Omega + 7.4 \text{ k}\Omega} = 3.3 \text{ V}$$

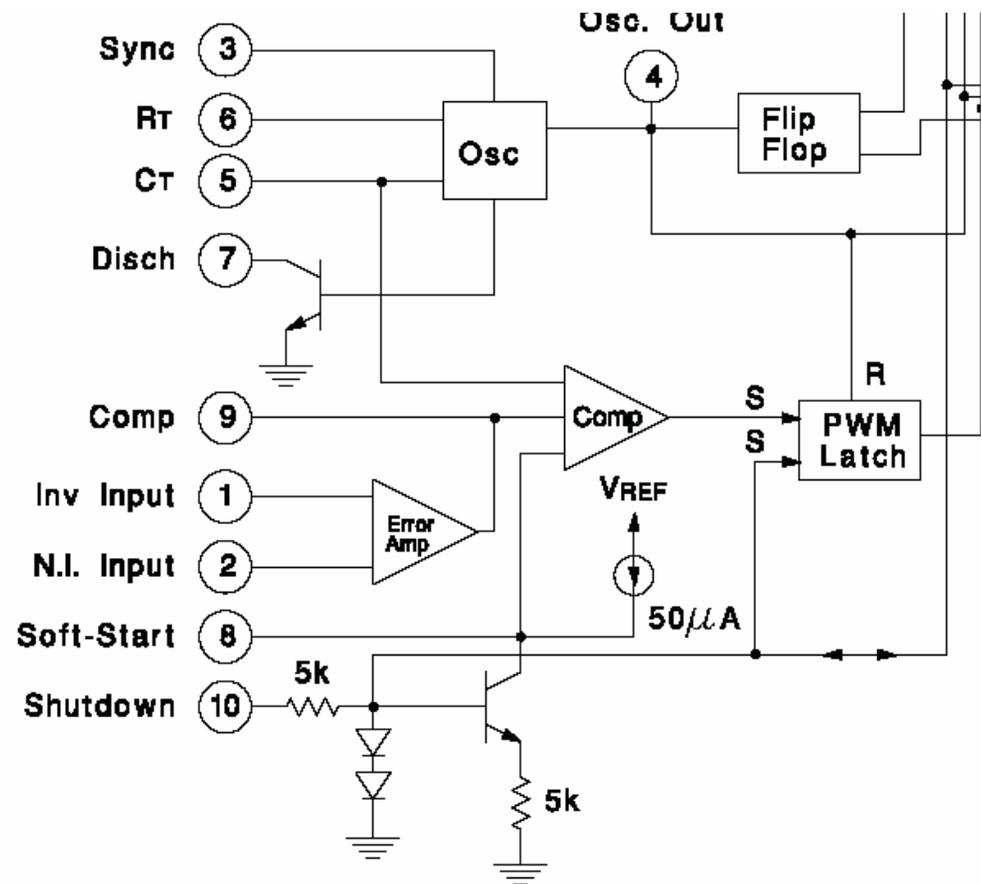
$$V_{\min} = (5.1 \text{ V}) \frac{(2 \text{ k}\Omega \parallel 14 \text{ k}\Omega)}{(2 \text{ k}\Omega \parallel 14 \text{ k}\Omega) + 7.4 \text{ k}\Omega} = 1.0 \text{ V}$$

Blanking pulse causes driver outputs to be low, so that $dT_s \leq t_c$

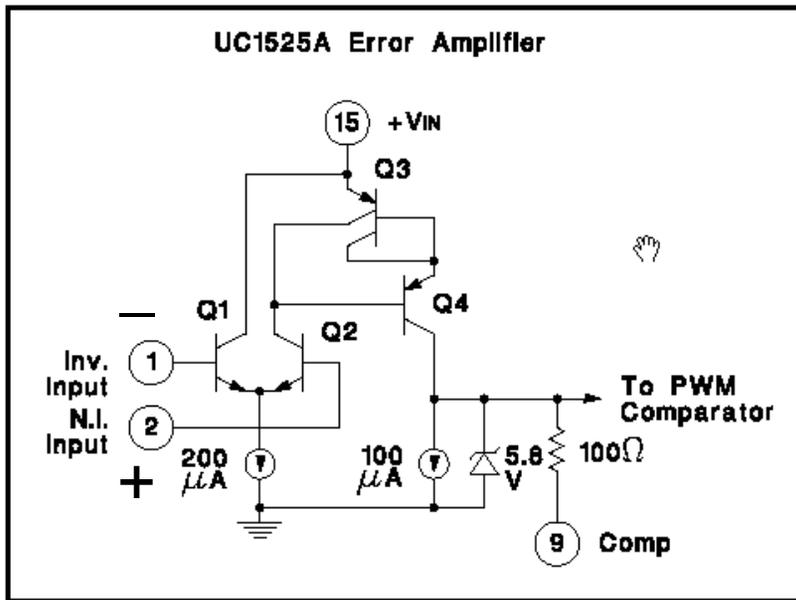
Increasing R_D reduces maximum allowed duty cycle D_{\max}

PWM Comparator and Latch

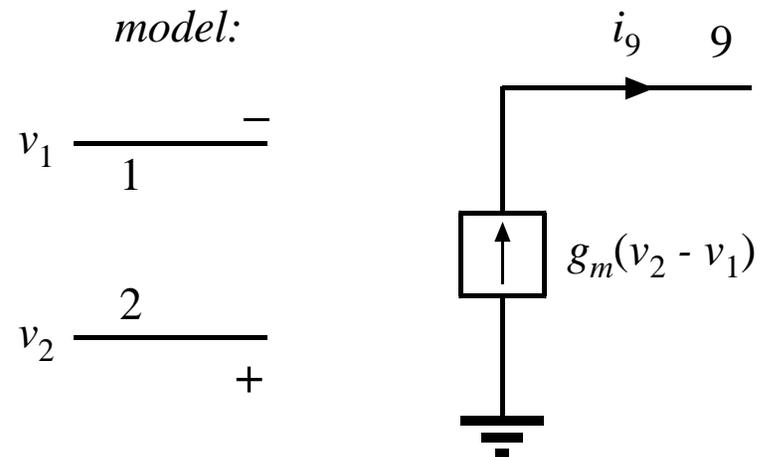
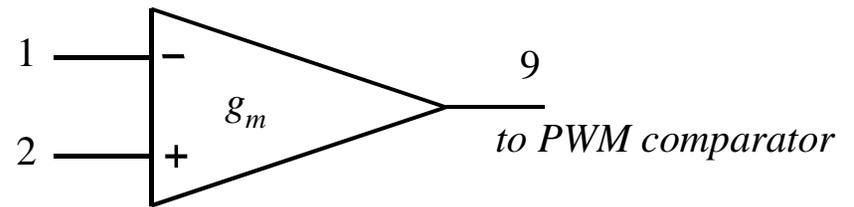
- PWM comparator "Comp"
- PWM latch is reset by oscillator during blanking interval, which starts the DT_s interval
- PWM latch is set by PWM comparator, which ends the DT_s interval
- The PWM latch prevents noise in the analog input from causing multiple switching during a switching period



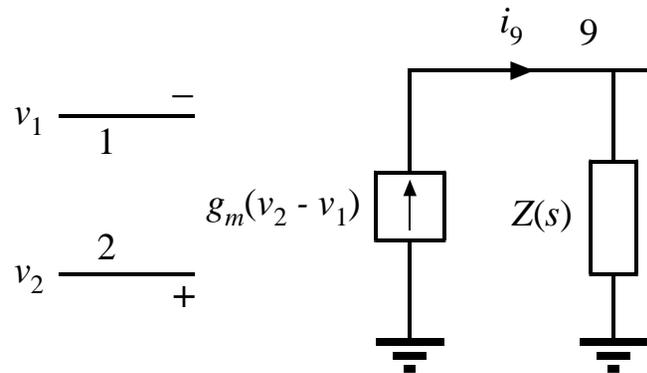
Error Amplifier



Transconductance amplifier



Error Amplifier with Load

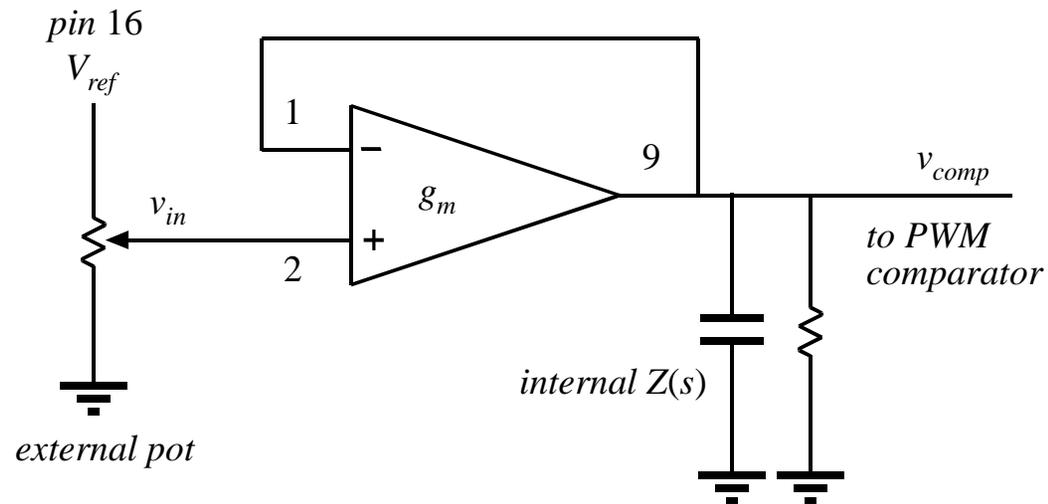


$$v_9 = g_m Z(s)(v_2 - v_1)$$

The differential voltage gain is: $g_m Z(s)$

With large $Z(s)$, the differential voltage gain is large. The data sheet specifies a low-frequency differential voltage gain of at least 1000 (60 dB).

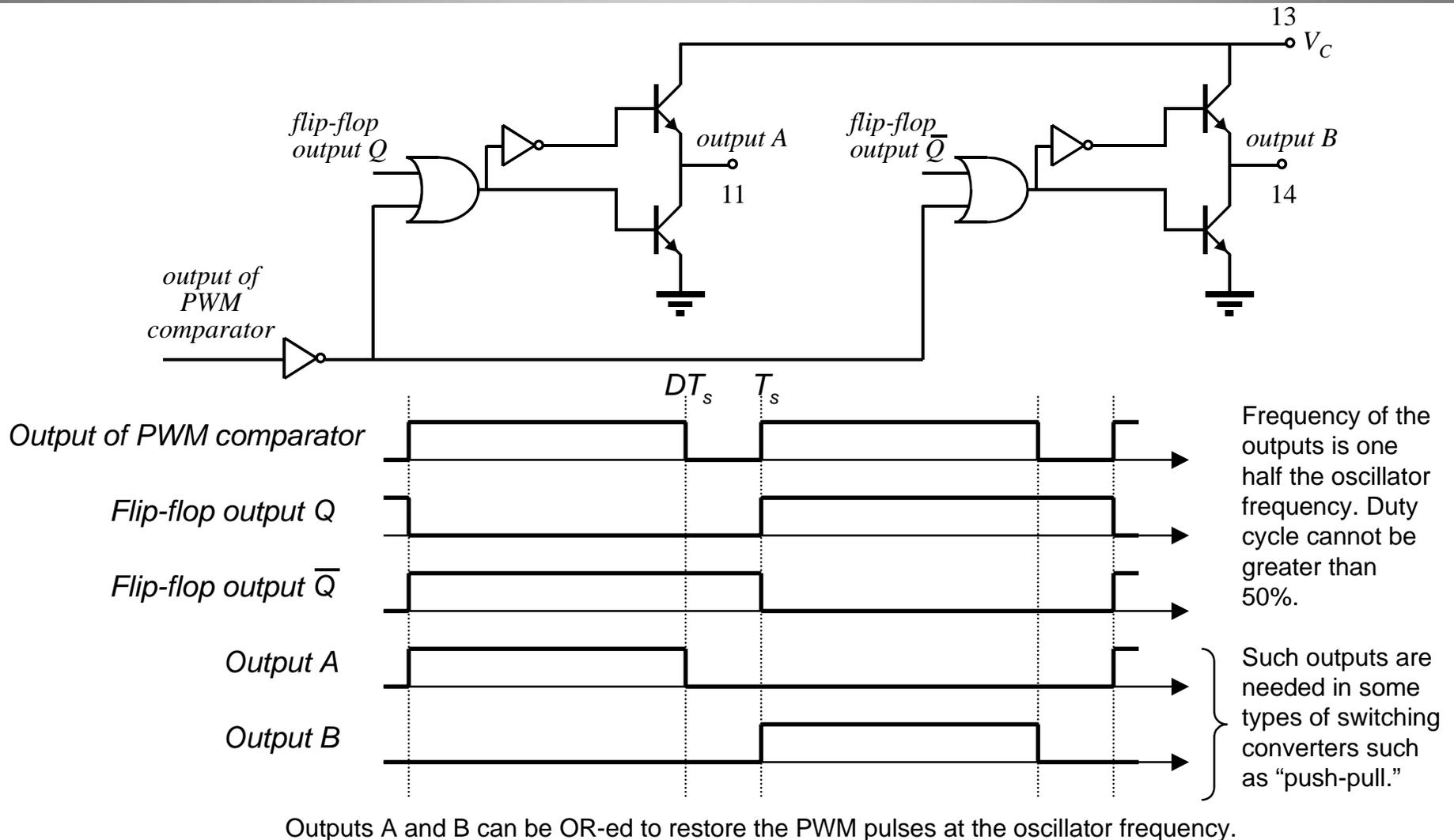
Connect to produce adjustable D



The error amplifier is connected as a unity-gain stage: $v_{comp} = v_{in}$

The duty cycle D can be adjusted by the external pot.

Outputs of the UC3525A



Soft start and shutdown

The shutdown pin (10) turns off the chip outputs. Ground this pin to ensure that the outputs are not shut down.

A capacitor can be connected to the soft start pin (8). The voltage on this pin limits the maximum duty cycle. At turn on, the capacitor will start at 0V, and then will charge from the 50 μ A current source. This overrides the feedback loop and starts the converter gently.

