Lecture 9
ECEN 4517/5517

Experiment 5

Buck converter
Battery charge controller
Peak power tracker
Due dates

This week in lab:
   Experiment 3 report (one from every group)
   Due within five minutes of beginning of your lab section

Next week in lecture:
   Midterm exam

March 31 in lecture:
   Exp. 5 prelab assignment

Late assignments will not be accepted.
Lab reports

• One report per group. Include names of every group member on first page of report.
• Report all data from every step of procedure and calculations. Adequately document each step.
• Discuss every step of procedure and calculations
  – Interpret the data
  – It is your job to convince the grader that you understand what is going on with every step
  – Regurgitating the data, with no discussion or interpretation, will not yield very many points
  – Concise is good
Goals in upcoming weeks
Exp. 5: A three-part experiment

Exp. 5 Part 1:
Demonstrate buck converter power stage operating open loop
Inside, with input power supply and resistive load
Outside, between PV panel and battery
DC system simulation

Exp. 5 Part 2:
Demonstrate open-loop control of converter from microprocessor
Demonstrate working sensor circuitry, interfaced to microprocessor
Demonstrate peak power tracker and battery charge controller algorithms, outside with converter connected between PV panel and battery
Exp. 5, Part 1
Demonstrate buck power stage inside
Gate drive circuit
with transformer isolation

- Gate driver output \( v_d(t) \) has a dc component when \( d \neq 0.5 \)
- Transformer will saturate if we apply dc
- Primary blocking capacitor removes dc component
- Secondary capacitor and diodes form a diode clamp circuit that restores the dc component
Gate driver transformer

- Use ferrite toroid in your kit
- Leakage inductance is minimized if bifilar winding is used
- Need enough turns so that applied volt-seconds do not saturate core:

$$\Delta B = \frac{V_1 DT_s}{n_1 A_c}$$
Alternate smaller version of gate driver

- Uses only one gate driver instead of two, to produce half the voltage swing on primary
- Transformer turns ratio is 1:1
- Produces half as much gate current
- Suitable for smaller MOSFETs
Exp. 5, Part 1
Test open-loop converter, outside

Basic control characteristics:

How does the duty cycle control the PV and battery voltages and currents?
Converter modeling and simulation

Conduction modes
  – Continuous conduction mode (CCM)
  – Discontinuous conduction mode (DCM)

Equivalent circuit modeling
  – The dc transformer model: CCM
  – DCM model

Simulation
  – Averaged switch model in CCM
  – Averaged switch model in DCM
  – A combined automatic model for PSPICE
Averaged switch modeling
Basic approach (CCM)

Given a switching converter operating in CCM

Buck converter example

Separate the switching elements from the remainder of the converter

Define the terminal voltages and currents of the two-port switch network
Terminal waveforms of the switch network

Relationship between average terminal waveforms:

\[
\langle v_1(t) \rangle_{\tau_s} = \frac{d'(t)}{nd(t)} \langle v_2(t) \rangle_{\tau_s}
\]

\[
\langle i_2(t) \rangle_{\tau_s} = \frac{d'(t)}{nd(t)} \langle i_1(t) \rangle_{\tau_s}
\]
Averaged model of switch network

\[ \frac{\langle v_1 \rangle}{d'} = \frac{\langle v_2 \rangle}{d} = \langle v_g \rangle \]

\[ \frac{\langle i_2 \rangle}{d'} = \frac{\langle i_1 \rangle}{d} = \langle i_L \rangle \]

So

\[ \langle v_1 \rangle = \frac{d'}{d} \langle v_2 \rangle \]

\[ \langle i_2 \rangle = \frac{d'}{d} \langle i_1 \rangle \]

Modeling the switch network via averaged dependent sources
PSPICE simulation
Exp. 5 Part 1: open loop

- Use your PV model from Exp. 1
- Replace buck converter switches with averaged switch model
- CCM-DCM1 and other PSPICE model library elements are linked on course web page
Sensing the battery current and voltage

Exp. 5 Part 2
ZXCT 1009 High-side current sense IC

Basic circuit for sensing current in a load

\[ V_{\text{out}} = I_{\text{load}} \frac{R_{\text{sense}} R_{\text{out}}}{100\Omega} \]
About the ZXCT1009

Power is supplied through the $V_{\text{sense}^+}$ and $I_{\text{out}}$ pins.

The IC is sensitive to negative-going signals or noise on the $V_{\text{sense}^+}$ and $V_{\text{sense}^-}$ pins.

Filtering the waveforms:

If necessary, a differential amplifier can be added to the microprocessor board, to obtain additional filtering and noise immunity.
Exp. 5 Part 3

- Implement maximum power point tracking algorithm
- Demonstrate on PV cart outside