HIGH-FREQUENCY ISOLATED 4kW PHOTOVOLTAIC INVERTER FOR UTILITY INTERFACE

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ABSTRACT

A utility interactive inverter based on high-frequency isolation has been developed by TESLaCo to generate a low-cost, compact, photovoltaic to utility interface at the residential power level of 4kW. A single quadrant, dc-isolated push-pull buck converter switching at 20 kHz is used to generate a full-wave rectified sine wave which is subsequently unfolded by a low-speed four-transistor bridge to result in a 60Hz sine wave power output. A control strategy optimizing the output impedance of the inverter for the direct interface to the stiff utility voltage has been developed. A novel peak power tracking circuit based on the inherent 120Hz input voltage ripple continuously follows the peak power without artificial operating point drift. Inverter shutdown after line disconnection is ensured even when the solar power input exactly matches a unity power factor load, fully protecting the servicemen. Despite its state-of-the-art low weight of only 17kg, the inverter is 92% efficient.

1. INTRODUCTION

With the cost of the conventional sources of energy such as oil and gas steadily increasing, and the cost of silicon and solar cells decreasing, the conversion of solar energy to electricity is rapidly becoming an economically viable alternative. However, the output of the solar cell is in the form of the direct current (dc) power, while most appliances and other electrical devices in residential use require an alternate (ac) power normally supplied by the utility. The required conversion to match the different kinds of source and load power can be realized by dc-to-ac inverters of two different types: stand alone inverter (SA) and utility interactive inverter (UI). The solar array power fluctuates considerably during each day depending on insolation level, weather conditions (clouds) etc. The residential load current also experiences extremely wide variations in the course of a day depending on actual usage of various appliances in the residence. Hence a need to balance the source and load power flow is created. As a first alternative, intermediate energy storage of solar power in an on-site battery may be utilized in conjunction with a stand alone (SA) inverter system. A stand alone system is one in which the inverter operates independently of the utility line; it never operates in parallel with the utility line and therefore must provide all power, both active and reactive that the residential load demands. Although this method is entirely feasible, fortunately there is a much simpler and more cost effective method which elegantly solves the power flow balance problem. In this so called Utility Interactive (UI) system, the inverter operates in parallel with the utility line to supply a common residential load as illustrated in Fig. 1. In this method the already available utility distribution ac system is used to balance the power flow between the dc source and ac residential load. For example, if, as shown in Fig. 1, the solar power input is greater than the ac power needed by a single residential load, the excess power is fed to the utility for further distribution to other residential loads. Analogously, if the solar power

Fig. 1. Solar photovoltaic to electrical power conversion using a utility interactive dc to ac inverter with unidirectional power flow: reactive power of the residential load is supported by the utility, while the excess active power is fed to the utility.

2. UTILITY INTERACTIVE INVERTER TOPOLOGY AND CONTROL STRATEGY

In this section a selection of inverter topology and semiconductor technology is made and the overall control strategy for successful intertie to the utility is reviewed.

2.1 Selection of the Inverter Topology and Semiconductor Technology

Today, a great number of converter and inverter topologies exist which can perform the required dc-to-ac inversion function. They range from the simplest one-quadrant converter to a full four-quadrant inverter power stage capable of handling non-unity power factor load and operating as a stand-alone unit. The cost and complexity of the design increases exponentially in the same direction. The older square-wave converter topologies based on low-frequency switching and filtering (60Hz-400Hz) are currently being displaced by modern high-frequency switching and filtering (typically at 20 kHz), thanks to the availability of fast, high-power switching devices, transistors and diodes. Not only are the size and weight of the units being reduced dramatically but, also, lower cost is made possible by de-emphasizing the materials cost of copper and iron, which are traditionally increasing in cost. The emphasis is then placed on semiconductor content (silicon), the cost of which is continuously going down.

Low cost and high reliability of the inverter requires the simplest possible topology that will still adequately fulfill the baseline specification requirements. The requirement for direct interface of the inverter to the utility line actually makes considerable simplification possible, and allows a single-quadrant converter approach.

2.1.1 Basic Conversion Technique

The essential features of the approach are shown in Fig. 3. The power processing is accomplished in two steps: in the first, the input dc from the solar array is converted into a series of half sine waves in the push-pull buck power stage; in the second, alternate half sine waves are inverted by unfolding stage to form the output complete sine wave that is matched to the 240V ac line (Fig. 3).

The first step is accomplished by a conventional push-pull quasi-square-wave converter operated in an unconventional manner. In normal use, such a converter would have its two switches closed alternately for a fraction of the 20 kHz switching period, and the rectified square-wave output would be filtered to remove the 20 kHz switching frequency and to recover the average, or dc, value that is proportional to the fractional on-time, or duty ratio, of the switches. In this application, in contrast, the duty ratio of the switches is modulated by a succession of 60Hz half sine waves (designated as AP sine waves in Fig. 3) in such a way that the rectified filtered output is no longer dc, but a reproduction of the 60Hz half sine wave control signal. The second step is accomplished by a straightforward transistor bridge, which inverts alternate half sine waves and generates the 60Hz full sine wave output.

At first, it may appear that the low frequency (60Hz) line-commutated switching is ideal for the output unfolding bridge to be implemented by silicon controlled rectifiers (SCR's). However, because of the intricacies involved in the direct interface to the utility line, especially under all possible fault conditions, and the drawbacks associated with reliable turn-off of SCRs, adoption of an all transistorized approach is much more attractive.

Fig. 3. Power stage and control block diagram of the TESLACo 4kW inverter.
The inverter system of Fig. 3 has excellent efficiency and cost-effectiveness. Although the power is apparently processed twice, the second step, the bridge inversion, is extremely efficient since the transistor drop is a small fraction of the line voltage, and there is essentially no switching loss. The overall efficiency is therefore essentially determined in the first conversion step, which is of a very straightforward and simple topology and contains only two switches. As a result, overall calculated efficiency of 92% should come as no surprise. A novel and simple way has been devised for preventing one of the problems inherent in push-pull converters, that of magnetic BH loop "creep" due to small asymmetries between the two sides [2]. This orthogonal flux sense winding circuitry designated by a cross sign on Fig. 3 maintains the absolute level of flux within the safe operating area of the transformer.

2.2 Overview of the Control Strategy

First, the main concept of the utility interactive inverter interface to the utility line is described.

Utility Interface

The reference rectified sine wave voltage is generated internally by digital circuitry and a D/A converter and is locked to the line by use of the digital phase-locked loop (PLL) circuitry. Current delivered to the line is automatically in phase with the voltage, once it is brought into synchronism with the line through the PLL circuitry. When a phase discrepancy between the line and reference signal is detected, the system shuts down and comes back on as soon as phase lock is reestablished. The RMS line voltage and its frequency are constantly monitored and an out of tolerance line will similarly cause the system to shut down, and then restart when proper line conditions return. Note also that the unfolding bridge transistors are controlled (turned on) by the signals generated from zero-crossings of the PLL sine wave. Consequently, well defined and noise free control of the unfolding stage is obtained.

The question always arises in this kind of application as to what is the distortion of the 60Hz output. Actually, what is important is not the distortion in the generated voltage per se, but the distortion in the current waveform delivered to the line by the inverter. With this understanding, it follows that an inverter that generates a perfect sine wave of voltage would deliver a perfect sine wave of current only into a line that already has a perfect sine wave of voltage; otherwise, if the line has distortion already present, the current delivered will also be distorted.

There are basically three approaches to controlling the ac inverter output when interfacing to the utility.

a. Making the inverter look like a low impedance sinusoidal voltage source.

b. Making the inverter look like a high impedance sinusoidal source.

c. Making the output current of the inverter be proportional to the instantaneous line voltage, so that it effectively follows the line.

The approach finally adopted is a combination of (a) and (b) so as to obtain some of the best features of both. The result is an inverter with a resistive output impedance (6Ω for a 4kw unit) so that large harmonic currents are not generated in the presence of minor line distortions, but yet the inverter will make some effort to restore the waveform of a badly distorted line.

Approach (c) has serious problems, in that it presents a negative resistance to the line, so it is likely to oscillate with various line impedances. An inverter with such a control scheme would also act so as to reinforce line deformities, which is certainly not a desirable outcome.

The desired output resistance of the inverter is obtained by purely active means; there is no actual dissipative resistor in the circuit, and any voltage imposed on this output resistance does not result in circuit losses.

This controlled active output resistance is obtained by use of current feedback in the buck converter stage, described in more detail in Section 3.1.2.

A short description of the function of various blocks in the inverter diagram of Fig. 3 follows, while the more detailed explanations are contained in later sections.

Buck PWM Control

This part generates the PWM base drive signals. The circuit also measures the switch current and uses this signal for both overload protection and for current feedback. The current feedback allows the output impedance of the converter to be precisely controlled. For the 4kw prototype, it is used to make the output impedance be 6Ω, resistive up to high frequencies (≈ 4 kHz). This maintains a relatively "soft" line interface and eliminates large harmonic currents in the presence of a distorted line.

Unfolding Transistor Control

Controls the output transistor bridge and monitors the current in each of the 4 transistors. In ac fault conditions, when the buck stage rectifier combined with the unfolding transistors may appear as a short on the ac line, the output stage protection circuitry rapidly turns off the unfolding transistors to protect them from damage, and a fault signal is sent to the central control logic.
**Output Current Feedback Control**

This circuit measures the average ac output current of the system and modulates the signal to the buck control circuit so as to maintain it at the desired level. This control is relatively slow, with a response time of approximately 2 seconds.

**Peak Power Tracker**

The peak power point is determined dynamically by use of the small amount of 120Hz ripple voltage imposed on the array. This scheme does not need readjusting for different array types or operating conditions, as it actively determines the optimum operating point.

**Bias Supply**

A multiple-output low-power (20W) switching power supply using a dc-isolated, coupled-inductor Cuk converter provides all the voltages needed for the control circuitry and basic drives.

Finally, a simplified block diagram of the feedback structure in Fig. 4 shows the flow and interrelationship of major control loops and protective features. The output of the buck stage is derived from a digitally generated sine reference produced by a PLL circuit that locks into the 60Hz line. During normal operation, the input voltage control circuit acts so as to null the error signal from the peak power tracker. However, when the array peak power point lies above 240V or below 160V, the peak power tracker error signal is overridden so as to maintain the array voltage between these limits. The peak power tracker is also overridden if the current into the 240V ac line exceeds 17A rms (corresponding to 4kW). In this situation, the array voltage is increased to a level greater than the voltage corresponding to peak power point until the output current is within 17A rms. In this mode, the input voltage may be allowed to go up to at least 250V before the inverter shuts itself off.

A photograph of the 4kW inverter is shown in Fig. 5 with its front panel removed to display the placement of major components. The size of the unit can also be easily envisioned when compared with the enclosed inch ruler.

3. **UTILITY INTERACTIVE INVERTER DESIGN**

3.1 **Buck Stage**

3.1.1 **Buck Power Stage Design**

The function of the push pull buck stage is to convert the dc power from the solar panel into a full wave rectified sinusoidal waveform that needs only to be inverted at every zero crossing (by the unfolding stage) to produce the desired 240V 60Hz output. The buck stage shown in Fig. 6 performs this function as well as providing isolation between the dc and ac sides of the circuit. This isolation is obtained through the use of a 20 kHz transformer, which can be made very compact and light (1.2kg) as opposed to about 25kg for the equivalent 60Hz 4kW transformer.

![Fig. 4. Gain-block diagram of the inverter control circuitry.](image-url)
Fig. 5 Photograph of the TESLACo inverter with its front panel removed.
The two power transistors are switched at a constant 20 kHz, and their duty cycle is modulated so as to produce the desired output waveform. Since the output waveform needs to vary between 0 and 350V the transistors have to be controlled down to very low duty ratios for a clean zero crossing. The base drive scheme used for this purpose is shown in Fig. 7. The circuit used is basically a proportional base drive with a β of 25, but the current transformer is disconnected during the turn off portion of the cycle. This is done to allow the base to be pulled to -6V, even after a very brief on time (<500ns) without fear of saturating the base drive transformer before the transistor has been completely turned off. When used with this rather hefty base drive (I_{b2} = 20A peak) the GE D67 darlington transistors can be made to switch quite quickly. When switching 65A into 200V they have a storage time of only 1.5μs and a fall time of 300ns. At low currents and duty cycles the storage time becomes negligible, allowing precise control of the output zero crossings. The main power transformer is built on a ferrite core (TDK EI090) and is wound with interleaved copper foil so as to obtain a very low primary to secondary leakage inductance of < 200nH, as measured from either primary winding. With this tight coupling almost no snubbing is needed, allowing for high efficiency operation.

3.1.2 Buck Power Stage Control

A block diagram of the control structure used is shown in Fig.6 and is rather unusual in that it uses voltage feedforward (ramp height modulation) coupled with current feedback. Voltage feedforward rather than feedback is used for two reasons:

Fig. 6. Buck stage circuitry.

first, it has the advantage of having virtually no dynamics, and unlike voltage feedback it is completely insensitive to the output load impedance. In the case of a utility interactive inverter this is very important since the output must be stable when the inverter is operating into a wide variety of ac lines, which may have a whole range of different impedances. The second advantage of feedforward in this application is, that unlike feedback, it requires no special isolation in the control circuitry. The purpose of the current feedback is to provide the inverter with a synthesized, non dissipative, resistive output impedance. This controlled output impedance is essential, as it allows the inverter to try to correct distortion in the ac line waveform, while keeping the harmonic currents within reasonable limits. A block diagram illustrating the operation of the current feedback is shown in Fig. 8. From Fig. 8 we have
Thus the low frequency output impedance desired can be obtained by choosing an appropriate gain for the current return path. Note that in the actual control circuit (Fig. 6) that the current measured is the collector current rather than the actual output current. During the transistor on time these two differ only by the turns ratio of the power transformer. The current feedback is designed so as to produce a 6Ω output impedance for the inverter, which, at 4kW output corresponds to about 100V of "padding" between the amplified reference signal and the 240V ac line. A suitable model for the output impedance of the inverter is shown in Fig. 9. Note that the 6Ω output resistance will help to damp the resonance of the output filter. The measured output impedance of the whole inverter, including the noise filters following the unfolding stage, is shown in Fig. 10. The measurement confirms that the low frequency output impedance is approximately 6Ω. The second comparator in Fig. 6 is used to prevent the peak output current of the inverter from exceeding a level that it can safely handle. The auxiliary current limit loop will clip the output current in the case of sudden transients or a very distorted ac line.

The flux sense circuit of Fig. 6 actively maintains the volt-second balance of the power transformer using a method recently developed at Caltech [2]. The circuit uses a two turn orthogonal sense winding to directly measure the flux level in the transformer core, and then uses this signal to turn off the power transistors when the maximum safe level is exceeded. This method of maintaining the volt-second balance allows the transformer to be fully optimized for efficient power transfer.

3.2 Input Voltage Control Loop

The dc input of the inverter is directly tied to the photovoltaic array, and bypassed by a large capacitor bank (6000μF), which takes most of the 120Hz ripple current. For the purpose of the following analysis the power loss in the inverter circuitry will be neglected, so the inverter input power will be assumed to be equal to its output power. The inverter circuitry incorporates accurate feedforward compensation, which means that its input power is independent of the array voltage. The magnitude of the ac output current is controlled by the voltage drop across the 6Ω inverter output impedance shown in Fig. 11. If the line voltage is assumed to be constant this voltage drop is entirely controlled by the digital sine reference amplitude control. The result is that the amplitude control directly determines the input power demand of the inverter. However, when the constant power input of the inverter is combined with the array output impedance the result is an unstable system, and additional feedback is needed to allow the inverter input voltage to be properly controlled, as is essential for array peak power tracking and maintaining the inverter input voltage within its design range.
\[ I_{in} V_{in} = P \] (4)

\[ V_{in} = \frac{P}{I_{in}} \] (5)

\[ R_{in} = \frac{dV_{in}}{dI_{in}} = -\frac{P}{I_{in}^2} \] (6)

Note that \( R_{in} \) is -ve, and its magnitude is minimum for low voltage, high power, and maximum for high voltage, low power. The range of values for this inverter is

\[-6.4\Omega > R_{in} > -\infty.\]

The array small signal output impedance is a function of the operating point, and can be considered to vary from 0 to \( \infty \), and is always positive. Note that if the array is operated at its peak power point its small signal output impedance is given by \( V_{array}/I = P/I^2 \) so it exactly cancels the the inverter's negative input resistance. A suitable small signal model of the inverter input and array is shown in Fig. 12. Determining the characteristic equation for the model of Fig. 12

![Fig. 12. Small signal model for array and inverter input.](image)

\[ \frac{1}{r_a} + sC - \frac{1}{R_{in}} = 0 \] (7)

\[ R_{in} + r_a R_{in} sC + r_a = 0 \] (8)

\[ s + \frac{r_{in} + r_a}{r_{in} C} = 0 \] (9)

or

\[ s + \frac{R_{in}}{r_{in} C} = 0 \] (10)

This implies a right half plane pole for \( r_a > (-R_{in}) \) and shows that the system will be unstable whenever the array is operated below its peak power point.

This situation would be unacceptable for even the peak power tracking function as any small overshoot of the power tracker could lead to a latch up condition for the inverter input. This problem could be overcome by eliminating the feedforward compensation in the buck stage, so as to get rid of the negative input impedance, but this would lead to increased distortion on the output, since the array ripple voltage would then affect the output waveform. The solution used is to add an auxiliary loop that controls the amplitude of the reference signal as a function of the input voltage. However this loop is only allowed to update the amplitude of the reference at every zero crossing of the line voltage. The result is that during a single 60Hz cycle the inverter is entirely controlled by its internal loops (feedforward and current feedback) and the properties discussed in the previous section. However, in the long term (over several cycles) its output is controlled by the voltage control loop, and the other feedback paths that feed this loop.

![Fig. 13. Small signal model of the input voltage control loop.](image)

For the initial analysis the sample and hold circuit will be ignored, a small signal model of the input voltage control loop is shown in Fig. 13. The \( V_{b} \) voltage source is an artificial voltage used in the model to control \( I_{in} \). In the actual circuit \( P \) or output power is the only quantity that can be directly controlled (by varying the reference amplitude) and gain \( k_2 \) is determined by the parameters of the power circuitry. Determining the characteristic equation for the closed loop system in equation (11)

\[ \frac{r_{in} + r_a}{r_{in} C} + \frac{1}{r_a} + sC = 0 \] (11)

\[ \frac{r_{in} + r_a}{r_{in} C} - (1 - k) \frac{r_{in} + r_a}{r_{in} C} = 0 \] (12)

\[ s + \frac{r_{in} + r_a}{r_{in} C} = 0 \] (13)

for a left half plane pole and a stable system the condition of equation 14 must be satisfied

\[ \frac{(1 - k) \frac{r_{in} + r_a}{r_{in} C}}{r_{in} C} > 0 \] (14)

since \( R_{in} < 0 \)

\[ (1 - k) \frac{r_{in} + r_a}{r_{in} C} < 0 \] (15)

\[ (1 - k) \frac{r_a}{|R_{in}|} < 0 \] (16)
since $r_a$ may be very large, to ensure stability

$$k > 1,$$ or $k_1 k_2 > 1$.

What is left is to evaluate the value of $k_2$ so that a desired design value of $k_1$ may be obtained. For a constant voltage $V_c$,

$$\frac{\dot{I}_{in}}{I_{in}} = \frac{-p}{1_{in}},$$

and

$$1 = \frac{-\dot{V}_b}{r_{in} I_{in}}.$$

This leads to equations (17) and (18)

$$\frac{\dot{V}_b}{r_{in}} = \frac{-p}{1_{in}}$$

(17)

$$\frac{\dot{V}_b}{V_c} = \frac{-r_{in} I_{in}}{p}$$

(18)

from (6)

$$r_{in} = \frac{-p}{1_{in}}$$

(19)

combining (6) and (18),

$$\frac{\dot{V}_b}{V_c} = \frac{1}{r_{in}} I_{in} = k_2$$

As it has been determined that $k_1 k_2 > 1$, the worst case occurs when $k_2$ is smallest, or $I_{in}$ is largest. Since $I_{in}(max) = 25A$, $k_2 \min = 40V kW^{-1}$. Thus to satisfy the condition $k_1 k_2 > 1$

$$k_1 > \frac{1}{k_2} = 25W V^{-1}$$

(20)

To have a comfortable safety margin $k_1 k_2 = 2$ is used, or $k_1 = 45W V^{-1}$. If one calculates the loop gain of the voltage control loop one obtains a maximum crossover frequency of 6Hz. The extra phase shift due to the sample and hold is then only 18°, and the final phase margin is 42°. Figure 14 shows a diagram of the final control structure in which the product $k_3 \dot{p}/\nu_m = k_1$, $\dot{p}/\nu_m$ is a simple combination $D$ to $A$ and buck stage stages. The closed loop transfer function $\nu/\nu_c$ varies considerably as a function of the combination $V_{in}/V_{in}$, but for the case when $r_d|\nu_m = \omega$, that is, when the array is being operated at its peak power point, the closed loop gain has a dc value of $1/k_3$ and a single pole at $\omega = k_1/C$. The value of $\omega/2\pi$ varies between 4.9 and 7.2Hz for $V = 160 \pm 240V$.

The final result is that there is a direct control available for the inverter input voltage, to which the other system controls may easily interface.

Fig. 14. Final implementation of the input voltage control loop.

3.3 Peak Power Tracker

The purpose of the peak power tracker [3] is to allow the photovoltaic array to be optimally loaded over the full range of operating conditions, so as to extract the maximum available electrical output power. The inverter is designed to follow the peak power operating voltage of the panel over the range of 160 to 240V.

The voltage at which the peak power point lies is determined by using the small amount of 120Hz ripple (= 5% pp max) present in the array to trace out a small portion of its IV characteristic. Since the IV curve is being measured at a relatively high rate (120Hz), conditions of rapidly changing insolation will not mislead the power tracker, as is likely with methods that use a slow artificially imposed dither to measure the array characteristic. Another disadvantage of artificial dither is that it forces the inverter periodically to deviate from the optimum voltage.

At the 120Hz frequency of the voltage ripple, the array impedance is large compared to that of the 6.000uf capacitor $C$ across the dc input of the inverter, so a suitable circuit model is that shown in Fig. 15. It can be shown that the ac component $\nu$ of the array voltage is

$$\nu = \frac{I}{2\nu C} \sin 2\omega t$$

(21)

Thus $\nu$ is positive in the intervals $0 \to 90^\circ$ (A) and $180^\circ \to 270^\circ$ (B), and negative for $90^\circ \to 180^\circ$ (C) and $270^\circ \to 360^\circ$ (D).

Fig. 15. Model used for determining the voltage ripple present on the array.
Fig. 16. Computer generated plots of the array characteristics.
The peak power tracker operates by determining the difference between the average array power in intervals (A) and (B) and the average power in (C) and (D). The comparison conditions are:

\[ P(\hat{V}^+) - P(\hat{V}^-) > 0 \] peak array power lies at a higher voltage

\[ P(\hat{V}^-) - P(\hat{V}^+) < 0 \] peak array power lies at a lower voltage

Figure 16 shows some computer generated plots of power and voltage ripple for various operating conditions.

The peak power tracker loop uses the \( P(\hat{V}^+) - P(\hat{V}^-) \) signal as an error signal to control the loaded array voltage. The error signal is then integrated and sent to the input voltage control circuit.

Rather than using an ordinary (expensive) analog multiplier to calculate the array dc power from the current and voltage signals, and ac coupling the output to obtain the \( \hat{p} \) signal, a lower cost alternative that needs no adjustment is used. The principle is to generate directly the \( \hat{p} \) signal by using the small-signal approximation of Eq. (22):

\[ \hat{p} = \hat{I}V + \hat{V}\hat{I} \]  

(22)

Note that both multiplications consist of one dc referenced quantity and one ac signal. This allows each multiplication to be performed by a low cost untrimmed transconductance amplifier. The bias input is used for the dc quantity and the differential input for the ac signal (input offset voltage does not matter since the differential input is ac). However, it is still important that the gains of the two multiplications be identical. This is ensured by switching one amplifier between the two multiplications with exactly 50% duty cycle. The result is that any gain variations do not affect the accuracy of the \( \hat{p} \) output, but only its magnitude. A block diagram of the peak power tracker is shown in Fig. 17.

Unfortunately the magnitude of the \( \hat{p} \) signal is a strong function of the power being drawn from the array and of the array voltage. So, if the output of this first multiplier were to be used directly, the final loop gain of the power tracker would vary unacceptably over the operating range of the inverter.

To solve this problem, let us take a closer look at the relationships between array voltage \( V \), current \( I \) and power \( P \). Using \( P = IV \) from (21) we have

\[ \hat{V} = \frac{I_{so}}{2\omega C} \sin 2\omega t = \frac{P}{2VC_{av}} \sin 2\omega t \]  

(23)

Since close to the peak power point the small-signal array resistance is

\[ r = \frac{V^2}{P} = \frac{\hat{V}}{\hat{I}} \]

\[ \hat{I} = \frac{\hat{V}}{r} = \frac{P^2}{2V^2C_{av}} \sin 2\omega t \]  

(24)

\[ \hat{V} = \frac{\hat{F}^2}{V^2} \cdot \frac{2\omega C}{\sin 2\omega t} = \frac{\hat{V}}{\hat{I}} \]  

(25)

Equation (25) implies that \( \hat{p} = 0 \), as one would expect for small signal \( \hat{v} \) near the peak power point.

The gain of the second multiplier in the circuit of Fig. 17 is controlled by an agc loop that maintains a constant magnitude of the \( IV \) or \( VI \) signal, whichever is larger. Near the peak power point, where \( IV = VI \), the gain \( k \) of the multiplier and agc circuit combined may be expressed as

\[ k = \frac{|V_{agc}|}{2|IV|} \]  

(26)

Fig. 17. Block diagram of the peak power tracker.
where $|V_{agc}|$ represents the peak voltage at the agc output, and the factor of $2$ in the denominator is the result of the 50% duty cycle for each multiplication. This signal, which contains the $\hat{p}$ information, is then fed to a synchronous detector for which the average output $\langle D \rangle$ over a 120Hz cycle is given by

$$\langle D \rangle = \hat{p} \frac{2}{\pi}$$  \hspace{1cm} (27)

![Diagram showing the small signal slope used for the stability analysis.]

**Fig. 18. Array IV curve showing the small signal slope used for the stability analysis.**

$$p = \frac{P}{rVc} \sin 2\omega t \Delta V$$

which, with $r = V_o^2/P$, becomes

$$\hat{p} = \frac{p^2}{v_o^2} \sin 2\omega t \Delta V$$

Since, for small signal conditions, $V_o = V$, this becomes

$$\hat{p} = \frac{p^2}{v_o^3} \Delta V$$

$$|\hat{p}| = \frac{p^2}{v_o^3} \Delta V$$  \hspace{1cm} (31)

The final gain for voltage error $\Delta V$ to average detection output voltage $\langle D \rangle$ is obtained by combining (27) and (31):

$$\frac{\langle D \rangle}{\hat{p} \Delta V} = k \cdot \frac{2}{\pi} \frac{p^2}{v_o^3 \omega C}$$  \hspace{1cm} (32)

with (26),

$$\frac{\langle D \rangle}{\Delta V} = \frac{|V_{agc}|}{2V_o} \cdot \frac{2}{\pi} \frac{p^2}{v_o^3 \omega C}$$

and then with (25),

$$\frac{\langle D \rangle}{\Delta V} = \frac{|V_{agc}|}{2V_o} \cdot \frac{2}{\pi} \frac{p^2}{v_o^3 \omega C} \frac{p^2}{v_o^3 \omega C}$$

so that finally

$$\frac{\langle D \rangle}{\Delta V} = \frac{2|V_{agc}|}{\pi V}$$

(35)

This final result represents a very usable signal, as it is independent of power level and varies only with $1/V$ which, over the 160 to 240V operating range, is a relatively minor effect. For a nominal input voltage of 200V, and $|V_{agc}|$ of 1.5V, the gain $\langle D \rangle/\Delta V$ is 4.3V V$^{-1}$ and this is the gain of the signal that is fed to the integrator which controls the input voltage. The entire loop has a response time of approximately 1.25 seconds from 1/3 to full power; below 1/3 power, the agc comes out of regulation and the loop is slower, but works properly to below 1/10 of maximum input power.
3.5 Line Locking Phase Locked Loop and Stability Considerations

The phase locked loop circuitry of the inverter has several tasks to accomplish. Its primary function is to generate a sine wave reference voltage in phase with the 240V ac line. An equally important function of PLL is to detect when the line deviates from its nominal frequency or voltage by more than a preset value and then to initiate the orderly converter shut-down. From this, one may be led to believe, that the absence or disconnection of the line voltage will be easily detected leading to inverter shut-down. This is of course a necessary requirement for the protection of the repairmen working on a faulted line disconnected from utility company supply for service. This phenomenon, however, requires a much closer examination.

To simplify the explanation process, the inverter is assumed capable of bidirectional power flow. Consider first the case of the nonunity power factor load as shown in Fig. 20a. Note that before the line disconnection, the reactive load was supplied from the utility. Upon the line disconnection, the output voltage will be shifted in phase from the inverter's internal equivalent voltage source, thereby producing the phase shift as seen in Fig. 20a. This phase discrepancy will be ultimately detected by PLL as a shift in frequency beyond the preset limit and result in inverter shut down. If, as in our case, the unidirectional inverter power flow applies, the same phenomenon occurs except with somewhat distorted waveforms.

Consider now the case of the unity power factor load as shown in Fig. 20b, for which no phase shift can be observed upon the line disconnection. However, if now the array power is larger than the active load demand, the output voltage will increase (dotted line). If the specified voltage limit is reached, the inverter will again shut-down and the line will be deenergized. Similarly, for load power exceeding array power, an undervoltage is detected and the converter is shut down.

However, anywhere in between the two voltage limits and even worse, when the solar input power just matches the load power (solid line in Fig. 6) neither the voltage nor the frequency shift would be detected, the inverter will continue running, thus still keeping the high voltage on the utility line. Obviously, a remedy for such a condition must be found to protect the utility repairmen.

The utility interactive inverters until now all had a basic operational flaw in that they would continue running when load power factor was approaching unity and was matched to the solar array power. TESLaco has found a solution to this problem by a relatively simple modification of the PLL circuitry which destabilizes the loop upon line disconnection and ultimately results in inverter shut-down.

Fig. 20 Effect of utility line disconnection: 
(a) finite phase shift for nonunity power factor load 
(b) zero phase shift for unity power factor load

A block diagram of the PLL circuits is shown in Fig. 21. The phase comparator used is a digital edge-triggered type with a precise 0° locking angle. In order to make it less susceptible to spikes and distortion on the ac line, it is preceded by an integrator, and for the whole circuit to have a locking angle of 0° one needs to compensate for the 90° phase shift of the integrator. This is accomplished by decoding the 90° address of the EPROM clock. The loop filter uses an ordinary lead-lag network for phase compensation, and is designed for a crossover frequency of 4Hz. This relatively low design frequency is used because of the 1.00 cycle time delay (shown shaded). Although this one cycle delay produces no locking angle error at exactly 60Hz, it does introduce a transport delay in the control loop, so a suitably low crossover frequency must be used for an acceptable phase shift. With the 4Hz crossover and a 70° lead network the final phase margin (including the time delay) is 45°. The purpose of the 1.00 cycle time delay circuit is to ensure that the PLL will be unstable when the ac line is disconnected. It also turns out that it can be used for the purpose of precisely measuring the line frequency. Under free run conditions, the line sense transformer is essentially connected directly to the digital sine generator via the power stage of the inverter, as shown by the dashed lines in Fig. 21.
When analyzing the response of the phase-locked loop one must remember that there are two different frequencies and phases of interest: the nominal line (60Hz) frequency $F_L$ and phase $\phi_L$, as well as the frequency and phase of the modulation signal $F_M$ and $\phi_M$. Note that under free run conditions the reference and VCO frequencies are the same since they are directly connected. This allows the use of one quantity $F_L$ to describe all the line frequency signals. Although the portions of the circuit carrying line frequency signals do not affect $F_L$, they do affect $\phi_L$, which represents the modulation $M$. For each of these sections the modulation gain can be written as:

$$\frac{M_{\text{out}}}{M_{\text{in}}} = \frac{d\phi_L}{dF_L}$$  \hspace{1cm} (36)

Note that this is a flat dc gain as far as the modulation signal is concerned. The only parts of the circuit that introduce any dynamics into the modulation transfer function are those parts of the circuit carrying VCO control signals, i.e. the loop filter. This may be analyzed using ordinary linear circuit methods.

A gain block diagram of the PLL circuits under free run conditions is shown in Fig. 22. What is left is to evaluate the loop gain $T$ by combining the individual gains. Note that the $d\phi/dF_L$ terms are additive since the total phase shift is the sum of the individual phase shifts, while the other terms are multiplied as usual.

$$T = (A_1 A_2 A_3)(A_4 + A_5 + A_6 + A_7 - A_8)$$  \hspace{1cm} (37)

$$T = \frac{2.1}{s}$$  \hspace{1cm} (38)

To obtain the characteristic equation (natural response) of the system, one sets $T = 1$ and the result is:

$$0 = 1 - \frac{2.1}{s}$$  \hspace{1cm} (39)

This corresponds to a right half-plane pole at 0.33Hz, and is an unstable system. This instability is just what is needed to ensure that the PLL frequency will drift off in the free run.
mode, and trip the frequency sense/phase lock circuit. Notice that if the 1.00 cycle time delay is not included, \( T = -0.11/s \), which corresponds to a left half-plane pole, and a stable system. From experimental measurements it has been confirmed that the system is indeed stable without the 1.00 cycle delay in the loop, and that it can be successfully destabilized with the addition of the time delay. The line frequency deviation from the 60Hz nominal is detected in a very simple manner by using an exclusive OR gate between the reference input of the phase comparator and the undelayed 90° VCO signal (Fig.21). If the phase comparator is locked at 0° and the frequency is exactly 60Hz, the output of the XOR gate will always be low, as its two inputs are exactly in phase. However, when the frequency changes, the time delay is no longer exactly one cycle, so the two signals are phase shifted by 6° for every Hz of deviation. The RC filter after the gate is designed so that the Schmitt trigger trips for any phase error greater than approximately 6°. As well as sensing frequency error this circuit will also detect an out-of-lock condition.

3.6 Inverter Start-Up and Shut-Down Sequencing

To protect the buck stage switches from dangerously high voltage switching, the base drives are directly disabled whenever the dc input voltage exceeds 260V. When the transistors are not switching, the voltage stress on them is reduced by a factor of 2, allowing them to withstand up to 500V dc input voltage.

In order to allow the inverter to start up into an array with an open circuit voltage greater than 260V, the array is initially shorted by R1 (for less than 10s) and the input capacitors are discharged by the resistor in parallel with R2. Relay R2 then opens, and as the array is charging the filter capacitors, the inverter begins to draw current from them, so the input voltage never reaches the array open circuit voltage. Relay R2 simply shorts the series diode during normal operation so as to avoid dissipating an extra 20W. Note that relay R1 does not have to be rated for high voltage dc switching because it is effectively snubbed by the input filter capacitors and the diode in parallel with R2. Relay R2 always opens before R1 closes, so it only switches 1 volt, and can also be quite small. A timing diagram showing the input switching sequence is given in Fig. 23.

![Fig. 23. Timing diagram for the inverter input turn-on and turn-off sequencing.](image-url)
4. PROTECTION FEATURES

In the design of the protection circuitry every effort was made to make the inverter immune from permanent damage for all likely fault conditions, and capable of restarting itself when conditions return to normal, without the need for any servicing (resetting breakers, replacing fuses, etc.). The inverter output side is protected against high voltage spikes by a 330 Joule Varistor. The four unfolding transistors are very wide safe operating area devices that can stand 900V and 90A simultaneously. In the case of a sudden ac line short or phase reversal, they will current limit at a safe 50A for a maximum time of 20us before being turned off by the control circuit. This protection is effective even with a zero impedance ac line, since the peak fault current is set by the protection circuitry, not the short circuit current of the 240V line. The inverter is designed to operate over an input range of 160 to 240V dc, but it can safely tolerate open circuit array voltages of up to 350V dc for extended periods. The limiting components are the input filter capacitors, not the semiconductors, as these are rated to 500V dc.

The inverter control logic differentiates between two types of error conditions. Type 1 errors result in the buck stage and unfolding transistors being turned off immediately so as to protect the inverter and the utility line against potentially dangerous conditions. Type 2 errors merely indicate that it is not desirable to operate the inverter when they occur, and when these errors persist for more than approximately 60s, the inverter will go into low power standby mode.

Type 1 errors: (immediate shutdown)
- Output (unfolded)
- Buck stage extreme overcurrent
- Line voltage out of tolerance
- Input overvoltage
- Excessive PLL phase or frequency error
- Heatsink over temperature
- Bias supply undervoltage

Type 2 errors: (standby mode)
- Input (array current) too low
- Line voltage out of tolerance
- Excessive PLL phase or frequency error

Some error conditions are listed in both categories, which means that these result in both immediate shutdown and eventually (after persisting for 60s) cause the inverter to go into standby mode.

5. PERFORMANCE EVALUATION

The collector-emitter voltage of one of the buck stage power transistors is shown in Figs. 24 through 27. These photographs were taken with an array voltage of 240V, and at full power, in an attempt to show close to the worst case operating conditions. Figure 24 shows two complete switching cycles close to the peak of the sine wave (high duty cycle). Note how the voltage spikes are quite small as a result of the very tight coupling of the power transformer. This allows the full VCE rating of the transistor to be used safely, because during turn off it only sees slightly more than the array voltage. If a transformer with more primary to secondary leakage were used, the turn off spike would be at least twice the array voltage. Figure 24 shows the transistor VCE for two cycles close to the sine wave zero crossing (low duty cycle).

Expanded turn-on and turn-off current and voltage waveforms are shown in Figs. 26 and 27. The turn-on current spike is due to the reverse recovery current of the output diode bridge. Note that the turn-on and turn-off crossover times are less than 500ns. Figure 28 shows the input voltage of the inverter as it starts up into a 4kW array with an open circuit voltage of 300V. One can see how the inverter begins to load the array before it reaches its open-circuit voltage. The small amount of 120Hz ripple impressed on the array by the inverter is clearly visible. Figures 29 and 30 show the array output current waveform into a relatively clean utility line. The current waveforms show the small glitches at zero crossings caused by the unfolding circuitry. Since the harmonic currents generated by the inverter are almost independent of the power level, the result is that the output waveform distortion is greater at lower power levels, as can be seen by comparing Figs. 29 and 30.

The three inverter prototypes built to date have been extensively tested in both our laboratory at TESLAco using an array simulator and at Sandia National Laboratories with an actual photovoltaic array. This rather thorough testing has enabled us to solve many initial design problems and incorporate the improvements in the present design. In order to properly test and design the peak power tracker and front-end of the inverter under easily controllable laboratory conditions, a wide bandwidth 5kW solar panel array simulator which accurately reproduces the array IV curve was developed and built at TESLAco. This has proved to be a valuable tool for refining the design of the inverter control circuitry.

The efficiency and distortion figures given in Table I were confirmed independently by Sandia National Laboratories and represent the actual performance of the entire system. The efficiency is measured from solar array dc input power to the final 240V ac output, and includes the effects of the internal bias supply, cooling fan, etc. The inverter run-on problem discussed in Section 3.4
Fig. 24 Buck transistor $V_{CE}$, at sine peak; 50V/div, 20µs/div.

Fig. 25 Buck transistor $V_{CE}$, close to sine zero crossing; 50V/div, 20µs/div.

Fig. 26 Buck transistor turn-on; 50V/div, 20A/div, 500ns/div.

Fig. 27 Buck transistor turn-off; 50V/div, 20A/div, 500ns/div.

Fig. 28 Inverter input voltage during start-up; 50V/div, 50ms/div.
was initially observed at Sandia National Laboratories and is experienced by several other manufacturer's inverters. When this problem was overcome by the modification of the phase-locked loop, our final design received further testing to ensure that this was indeed the case.

6. CONCLUSION

A number of approaches to photovoltaic inverters for utility interface are well known, ranging from low (400Hz) to high frequency (20 kHz) switching, and differing substantially in conceptual approach, choice of inverter topology, and detailed implementation. Naturally, their comparison shows a wide range of size, weight, cost and performance characteristics. Here several outstanding features of the TESLAc0 4kW, 20 kHz utility interactive inverter are highlighted.

1. The TESLAc0 4kW inverter is the first successful inverter based on the high-frequency isolation link PWM approach. Owing to 20 kHz switching, the isolation transformer weighs less than 1.2kg instead of 25kg as in conventional approaches. Consequently, the inverter weighs only 17kg in comparison to 50kg or more of the conventional approaches. Therefore, the inverter can be shipped via United Parcel Service within the USA since the total shipping weight is under 50 lbs. This not only ensures easier installation and servicing, but is also a much simpler, faster and cheaper way of delivery and handling for repair.

2. Low total harmonic distortion of less than 1.5% at full power level is due both to the high frequency link approach and to appropriate control strategy.

3. Complete removal of any possibility of the inverter continuing to run after the utility line is disconnected, in contrast to other inverters currently available which continue to run upon line disconnection when the solar array power is matched to a unity power factor load. This feature means complete safety to the repairman and user.

4. A novel approach for peak power tracking which utilizes the already available small 120Hz ripple voltage on the array input to inexpensively and continuously update the maximum power point.

5. A novel orthogonal flux-sensing technique which removes any possibility of the main isolation transformer saturation, since it detects the flux level instantaneously and turns the transistor switch off to equalize the volt-sec balance.

6. The main transistor switch is protected on a single cycle basis by use of a current sense transformer.

High efficiency of 92% at full power and 90% at half-power load and very low standby power of only 2.5W are also important features of the inverter design. The TESLAc0 unit was designed according to Sandia Baseline Specifications for Utility Interactive Power Conditioning for Residential Photovoltaic System [1]. Several versions of the unit have undergone extensive testing under extreme testing conditions at the Sandia testing facility in Albuquerque, New Mexico, and have performed satisfactorily for over 6 months.

The future design and optimization efforts will be directed toward further reduction of the cost of the inverter through component replacement.
and circuit upgrades. It is also anticipated that further testing may point toward additional new desirable features. One control board slot is at present left empty and is available for incorporation of future design modifications and optimizations of this first high frequency isolation link utility interactive inverter.

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REFERENCES

