Experiment 3

DC-DC converter
Battery charge controller
Peak power tracker
Due dates

This week in lecture (now):
   Exp. 3 prelab assignment (one from every student)

This week in lab:
   Exp. 2 scoresheet

Late assignments will not be accepted. Assignments are due within five minutes of beginning of period.
Goals in upcoming weeks
Exp. 3: A multi-week experiment

Exp. 3 Part 1:
Demonstrate dc-dc converter power stage operating open loop, driven by MSP430 PWM output
Inside, with input power supply and resistive load
Outside, between PV panel and battery
DC system simulation

Exp. 3 Part 2:
Demonstrate working sensor circuitry, interfaced to microprocessor
Demonstrate peak power tracker and battery charge controller algorithms, outside with converter connected between PV panel and battery
Exp. 3, Part 1
Demonstrate dc-dc power stage inside

Buck converter

- $V_g$: 0-35 V supply
- $C_1$: 3300 µF 35 VDC
- $Q_1$: HUF75321
- $i_T$: inductor
- $i_{C1}$: capacitor
- $i_D$: diode
- $i_L$: inductor
- $L_1$: inductor
- $v_D$: voltage
- $D_1$: MBR1645
- $C_2$: 330 µF 25 VDC
- $V$: output voltage

Other components:
- +12 V supply
- MSP430
- TC4428 gate driver
- 1N4148 zener diode
Exp. 3
Minimum timetable

This week
- Assemble power stage and gate driver on perf board

Next week
- Get circuitry working inside lab
- Take measurements outside

Third week
- Perform simulations
- Build sensor circuitry (Part 2)

Fourth week
- MPPT coding
- Demonstrate operation outside
Layout issues

Example: Buck converter

Use loop analysis

Switched input current $i_1(t)$ contains large high frequency harmonics
—hence inductance of input loop is critical
Inductance causes ringing, voltage spikes, switching loss, generation of B- and E-fields, radiated EMI

The second loop contains a filter inductor, and hence its current $i_2(t)$ is nearly dc
—hence additional inductance is not a significant problem in the second loop
Parasitic inductances of input loop explicitly shown:

Addition of bypass capacitor confines the pulsating current to a smaller loop:

high frequency currents are shunted through capacitor instead of input source
Even better: minimize area of the high frequency loop, thereby minimizing its inductance

B fields nearly cancel

loop area $A_c$
Example: gate driver

- Line input
- +15 volt supply
- Analog control chip
- PWM control chip
- Gate driver
- Power MOSFET

$i_g(t)$
Solution: bypass capacitor and close coupling of gate and return leads

High frequency components of gate drive current are confined to a small loop

A dc component of current is still drawn output of 15V supply, and flows past the control chips. Hence, return conductor size must be sufficiently large
Converter modeling and simulation

Conduction modes
- Continuous conduction mode (CCM)
- Discontinuous conduction mode (DCM)

Equivalent circuit modeling
- The dc transformer model: CCM
- DCM model

Simulation
- Averaged switch model in CCM
- Averaged switch model in DCM
- A combined automatic model for PSPICE (or Simulink, optional)
Averaged switch modeling
Basic approach (CCM)

Given a switching converter operating in CCM

Buck converter example

Separate the switching elements from the remainder of the converter

Define the terminal voltages and currents of the two-port switch network
Terminal waveforms of the switch network

Relationship between average terminal waveforms:

\[
\langle v_1(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle v_2(t) \rangle_{T_s}
\]

\[
\langle i_2(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle i_1(t) \rangle_{T_s}
\]
Averaged model of switch network

\[
\frac{\langle v_1 \rangle}{d'} = \frac{\langle v_2 \rangle}{d} = \langle v_g \rangle
\]

\[
\frac{\langle i_2 \rangle}{d'} = \frac{\langle i_1 \rangle}{d} = \langle i_L \rangle
\]

So

\[
\langle v_1 \rangle = \frac{d'}{d} \langle v_2 \rangle
\]

\[
\langle i_2 \rangle = \frac{d'}{d} \langle i_1 \rangle
\]
.subckt CCM1 1 2 3 4 5
Et 1 6 value=\{(1-v(5))*v(3,4)/v(5)\}
Vdum 6 2 0
Gd 4 3 value=\{(1-v(5))*i(Vdum)/v(5)\}
.ends
Basic CCM SEPIC Example
Frequency Response

Ideal SEPIC frequency response
.lib switch.lib
Vg 1 0 dc 120V
L1 1 2x 800uH
RL1 2x 2 1U
C1 2 3 100uF
L2 3 0 100uH
C2 4 0 100uF
RL 4 0 40
Vc 5 0 dc 0.4 ac 1
Rc 5 0 1M
Xswitch 2 0 4 3 5 CCM1
.ac DEC 201 10 100kHz
.PROBE
.end
PROBE Output
SEPIC Example: Control-to-output transfer function
Discontinuous Conduction Mode

- Again find average values of switch network terminal voltages and currents
- Eliminate variables external to the switch network
- Results on next slides
Input (transistor) port
Averaged equivalent circuit

\[ \langle i_1(t) \rangle_{T_s} = \frac{d_1^2(t) T_s}{2L} \langle v_1(t) \rangle_{T_s} \]

\[ \langle i_1(t) \rangle_{T_s} = \frac{\langle v_1(t) \rangle_{T_s}}{R_e(d_1)} \]

\[ R_e(d_1) = \frac{2L}{d_1^2 T_s} \]
Output (diode) port
Averaged equivalent circuit

\[
\langle i_2(t) \rangle_{T_s} = \frac{d_1^2(t) T_s}{2L} \frac{\langle v_1(t) \rangle_{T_s}^2}{\langle v_2(t) \rangle_{T_s}}
\]

\[
\langle i_2(t) \rangle_{T_s} \langle v_2(t) \rangle_{T_s} = \frac{\langle v_1(t) \rangle_{T_s}^2}{R_e(d_1)} = \langle p(t) \rangle_{T_s}
\]
Averaged modeling of CCM and DCM switch networks

**CCM**

- Switch network
  - $i_1(t)$
  - $v_1(t)$
  - $v_2(t)$

- Averaged switch model
  - $\langle i_1(t) \rangle_{T_s}$
  - $\langle v_1(t) \rangle_{T_s}$
  - $1 : d(t)$
  - $\langle i_2(t) \rangle_{T_s}$

**DCM**

- Switch network
  - $i_1(t)$
  - $v_1(t)$
  - $v_2(t)$

- Averaged switch model
  - $\langle i_1(t) \rangle_{T_s}$
  - $\langle v_1(t) \rangle_{T_s}$
  - $R_c(d_1)$
  - $\langle i_2(t) \rangle_{T_s}$
  - $\langle v_2(t) \rangle_{T_s}$
  - $\langle p(t) \rangle_{T_s}$
Spice model CCM-DCM1
Combined CCM/DCM switch model

*******************************************************************************
* MODEL: CCM-DCM1
* Application: two-switch PWM converters, CCM or DCM
* Limitations: ideal switches, no transformer
*******************************************************************************
* Parameters:
  * L=equivalent inductance for DCM
  * fs=switching frequency
*******************************************************************************
* Nodes:
  * 1: transistor positive (drain of an n-channel MOS)
  * 2: transistor negative (source of an n-channel MOS)
  * 3: diode cathode
  * 4: diode anode
  * 5: duty cycle control input
*******************************************************************************
.subckt CCM-DCM1 1 2 3 4 5
+ params: L=100u fs=1E5
Et 1 2 value={1-v(4))*v(3,4)/v(u)}
Gd 4 3 value={(1-v(4))*i(Et)/v(u)}
Ga 0 a value={MAX(i(Et),0)}
Va a b
Ra b 0 1k
Eu u 0 table {MAX(v(5), v(5)*v(5)/(v(5)*v(5)+2*L*fs*i(Et)/v(3,4)))} (0 0) (1 1)
.ends
*******************************************************************************

- This is one of the models inside switch.lib
- It automatically switches between CCM and DCM as necessary
PSPICE simulation
Exp. 3 Part 1: open loop

• Use your PV model from Exp. 1
• Replace buck converter switches with averaged switch model
• CCM-DCM1 and other PSPICE model library elements are linked on course web page