

Experiment #5 Design of an FSK Data Modem

© 1997 Dragan Maksimović
Department of Electrical and Computer Engineering
University of Colorado, Boulder

In this lab assignment your task is to design a data modem using a frequency modulation technique called *frequency shift keying*. The phase-locked loop based on the CMOS 4046 chip tested in Lab #4 is the main building block of the modem.

Operation of an FSK data modem is described in Section 1. Design specifications are given in Section 2, with design considerations in Section 3. Laboratory tasks are described in Section 4. The prelab assignment is in Section 5.

1 FSK Data Modem

A block diagram of the system is shown in Fig. 1. The system consists of two modem units (1 and 2) linked through a single line. At first, the link in the lab will simply be a pair of wires – one for the signal, and one for the common ground. The most common example for an actual link between the modems would be through telephone lines. The actual signal path through the telephone line is much more complicated than the simple pair of wires in the lab, but the modem operating principles are nevertheless the same. Other real-world links may include RF or optical. After you finish the system design using the ideal pair-of-wires link, you can experiment with a simple free-space optical link.

Each modem has a transmitter and a receiver. The transmitter takes serial binary data T_x from a data source (typically from a computer serial port). The data is a sequence of logic 1's and 0's, as shown in Fig. 1. In the lab, for test purposes, we can generate the data from a lab pulse generator. Each bit of data, 1 or 0, lasts for Δt seconds. The data transmission speed $B_r = 1/\Delta t$, is called the baud rate in bits per seconds (bps). If the transmitted signal is periodic, such as it would be if obtained from a simple pulse generator, the maximum fundamental frequency f_s of the signal is obtained for the periodic sequence $\dots 010101\dots$,

$$(f_s)_{max} = \frac{1}{2\Delta t} = \frac{B_r}{2}. \quad (1)$$

Frequency-shift keying is a type of frequency modulation in which the frequency of the FM signal on the line is varied between two fixed levels, f_H and f_L . In the modems of Fig. 1, the binary T_x signal determines the frequency of the line signal. Logic 1 corresponds to f_H , and logic 0 corresponds to f_L . The FSK signal on the line is a waveform with frequency equal to f_H or f_L depending on the binary input T_x . The purpose of the frequency modulation is two-fold: first, it shifts the spectrum of the transmitted signal to a range within the passband of the link between the modems. For a standard telephone line, the passband is approximately between 300Hz and 4kHz, and so f_H and f_L are selected to be in this range. The second purpose of the frequency modulation is to allow data to be transmitted in both directions through the same line at the same time. This is accomplished by assigning one pair of frequencies (f_{HA} , f_{LA}) for the data transmitted

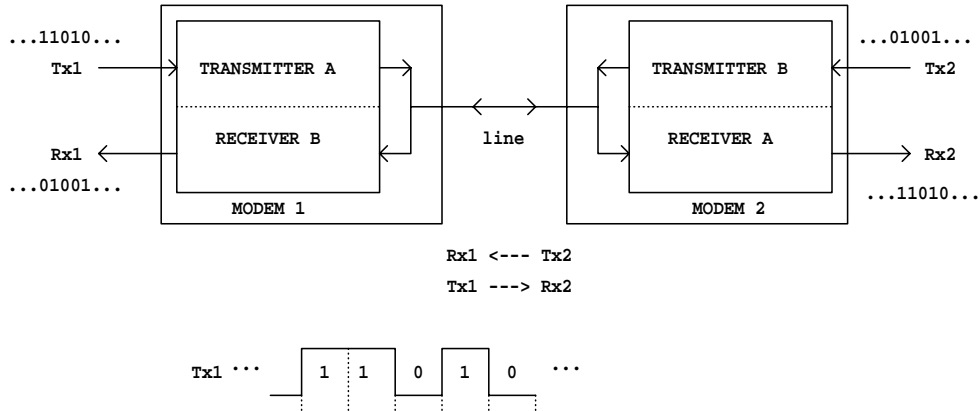


Figure 1: A block diagram of the system with two FSK modems.

from modem 1 to modem 2, and another pair (f_{HB} , f_{LB}) for the data transmitted in the opposite direction, from modem 2 to modem 1. Because of this assignment, each of the two signals uses about one half of the full bandwidth of the line, and the two signals can be transmitted, separated and demodulated independently. In communication theory, this technique is known as *frequency-division multiplexing*. The simultaneous data transmission in both directions over the same line is called *full duplex*. In Fig. 1, we can identify two communication channels: channel A, which corresponds to data transmission from modem 1 to modem 2, and channel B for data transmission in the opposite direction.

The receiver in the modem takes the signal from the line, extracts the portion that corresponds to the signal transmitted from the opposite side, and removes the portion that corresponds to the signal of the transmitter on the same side. Then, the receiver demodulates the incoming signal, generating logic 1 level when the incoming signal frequency is f_H , and logic 0 level when the incoming signal frequency is f_L . The received output is a binary sequence R_x , which is (if there are no errors) exactly the same as the original sequence T_x .

As shown in Fig. 1, each of the two modems (1 and 2) has a transmitter and a receiver. Ideally, if there are no errors, the R_{x2} sequence is the same as the T_{x1} sequence and R_{x1} is the same as T_{x2} .

1.1 Transmitter

A block diagram of the transmitter is shown in Fig. 2. The data source (a pulse generator) generates the signal T_x . The logic 1 and the logic 0 levels of T_x should be such that the corresponding frequencies at the output of the VCO are f_H (for logic 1 level) and f_L (for logic 0 level). The VCO output v_{osct} is the FSK signal. Before the signal is sent to the line, its dc component is removed by the capacitor in series, and its level is adjusted to the level allowed on the line by the attenuator ATT. Additional signal filtering would also be performed in the ATT block. The signal v_{it} is obtained at the low-impedance output of the transmitter. Finally, the line requires that the source has a standard source impedance, which in this case is $R = 1k\Omega$ (for phone lines it would actually be 600Ω). The signal on the line is v_{line} .

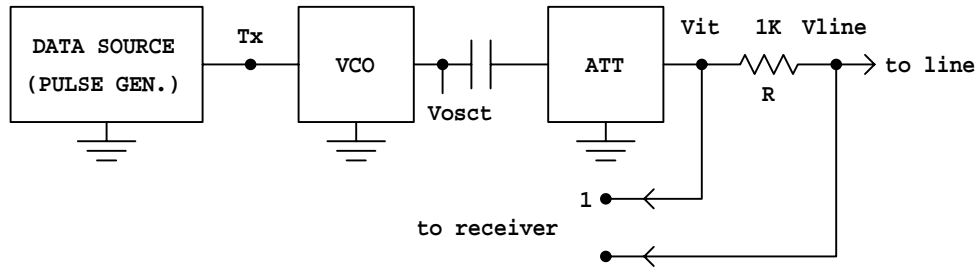


Figure 2: A block diagram of the FSK transmitter.

1.2 Receiver

A block diagram of the receiver is shown in Fig. 3. The line signal is terminated with the standard load $R = 1k\Omega$. Note that in one modem there is only one R , for both the transmitter and the receiver. The low-impedance transmitter output v_{it} can simply be connected to the other end of the load resistor R . The line signal is first passed through an op-amp based amplifier. The amplifier serves two purposes: to increase the signal level, if necessary, and to effectively cancel the modem's own transmitted signal v_{it} from the receiver. In addition, signal filtering would normally be implemented around or after the amplifier. The incoming FSK signal v_{ir} goes through capacitive coupling (to remove any dc components) to the input of the PLL. The PLL is the main component of the receiver – it performs demodulation of the FSK signal. However, even ideally, the output v_{or} is still not equal to the original binary signal T_x . First, v_{or} is affected by the dynamic response of the system, including the transmitter, the line, and finally the PLL. Second, v_{or} has a high-frequency ripple as a result of the PLL operation, as shown in lab #4. To get the final binary output, the PLL output v_{or} is passed through a voltage comparator that decides whether the received signal is logic 1 or logic 0.

1.3 Typical waveforms

Fig. 4 shows typical waveform expected in the system, starting from T_x to R_x , for a sequence example: $\dots 0100101\dots$. Note the FSK signal v_{ir} , switching between the two assigned frequencies f_H and f_L , as determined by the signal T_x . The waveform v_{or} shows a typical PLL output with the FSK signal input. The output v_{or} may have transient overshoots and ringing at each signal transition. The dynamic response is determined by the PLL parameters: K_o , K_D and the loop filter. In addition, v_{or} has a high-frequency ripple at the frequency $2f_L$, or at the frequency $2f_H$. Finally, with v_{or} at the input, the comparator makes the decision whether the signal is logic 1 or logic 0. Note that errors may occur if the ringing in v_{or} is too large, if the response is too slow, if the comparator threshold is not selected well, or if the ripple is too large.

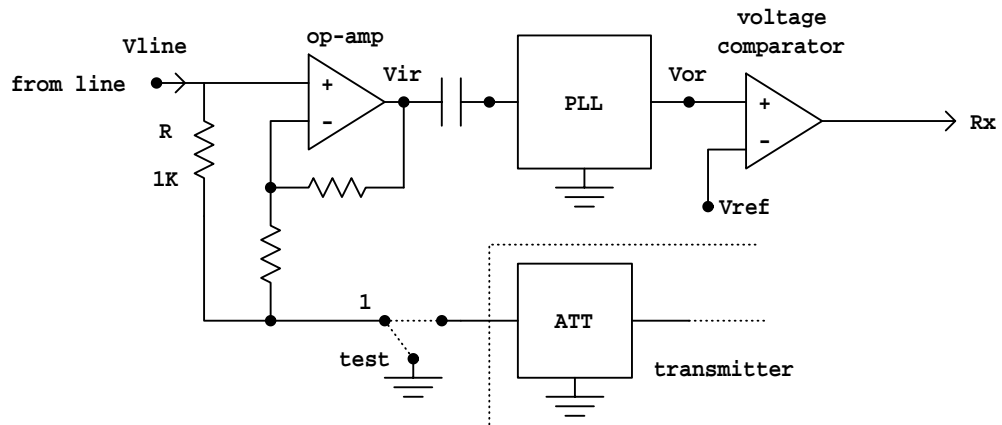


Figure 3: A block diagram of the FSK receiver.

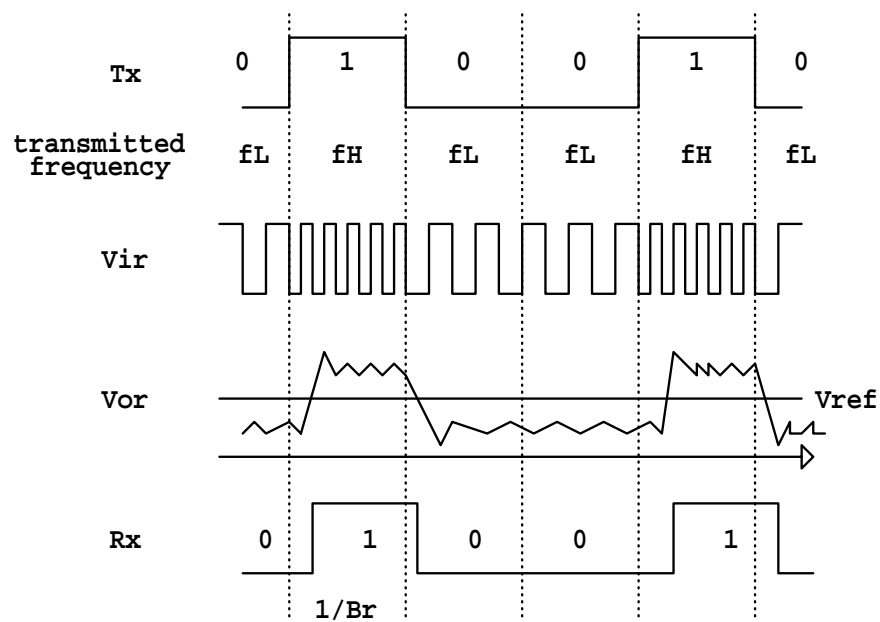


Figure 4: Typical waveforms expected in the system.

2 Design Specifications

Your task is to design one complete modem (just one, not both modems in Fig. 1) according to the following design specifications:

1. The FSK signal frequencies for the A-channel are:

$$f_{HA} = 10.5kHz \quad (2)$$

$$f_{LA} = 9.5kHz \quad (3)$$

2. The FSK signal frequencies for the B-channel are:

$$f_{HB} = 15.5kHz \quad (4)$$

$$f_{LB} = 14.5kHz \quad (5)$$

3. The minimum baud rate, with no errors, for both channels is $(B_r)_{min} = 500\text{bps}$. One of your tasks will also be to examine how high the baud rate without errors can be.
4. The line must be terminated by $R = 1k\Omega$.
5. The maximum allowed amplitude of the signal v_{line} that a transmitter outputs to the line (when the other transmitter is not active) is less than 1V peak-to-peak. Also, v_{line} must not have any dc component.
6. Supply voltages are +15V and -15V.
7. In addition to two 4046 chips (one for the transmitter, one for the receiver), other components you need for the design (such as op-amps and comparators) can be selected from the components used in the previous lab assignments.

3 Design Considerations

Here is a summary of main design considerations:

3.1 VCO in the transmitter

The VCO minimum and the maximum frequencies must satisfy $f_{max} \geq f_H$, $f_{min} \leq f_L$. The accuracy of f_L and f_H is important because the receiver will be easier to design and will be able to perform better (operate at higher baud rates without errors).

3.2 Attenuator in the transmitter

The ATT block can be designed around an op-amp. To determine the attenuation needed, consider the maximum allowed line signal amplitude. Since the VCO output is between 0 and +15V, you should include the capacitive coupling between the VCO output and the attenuator, in order to remove dc component from the line signal.

3.3 Input amplifier in the receiver

The amplifier can be built as shown in Fig. 3. Choose the gain so that v_{it} is ideally completely eliminated from v_{ir} when the point 1 is connected to the transmitter output v_{it} .

3.4 PLL in the receiver

The PLL design has two main components: selecting VCO parameters, and designing the loop filter. Results of lab #4 can be used in this part. These are the main considerations:

1. The lock range *and* the capture range must include f_H and f_L . To ensure that the PLL will lock reliably, you need to make sure that $f_L > f_o - f_c$ and $f_L < f_o + f_c$, where $2f_c$ is the capture range. The capture range depends on the filter characteristics, as examined in lab #4.
2. A low cut-off frequency f_p of the filter means that the capture range is small. Moreover, the system dynamic response can have high overshoots and long ringing. A high f_p on the other hand may result in too much ac ripple in v_{or} . In either case, detection of 0's and 1's without errors, using the voltage comparator at the output of the PLL, may be difficult to accomplish. You can experimentally determine a good trade-off. In addition, a more complicated loop filter configuration can be used to improve the performance. You can also consider placing a low-pass filter between the PLL output and the comparator.

3.5 Comparator in the receiver

The output of the comparator is the final output of the receiver, the binary signal R_x . As shown in Fig. 4, the comparator must resolve the signal at the PLL output. This signal is corrupted by both dynamic response of the system and by the high-frequency ac ripple. It is important to choose the threshold V_{ref} carefully. A hysteresis in the comparator characteristic can help to remove erroneous logic transitions at the comparator output, especially when higher baud rates are attempted.

4 Experiment

The main task in the laboratory is to design and test the basic system as shown in Fig. 1.

Instead of the usual set of laboratory instructions, this section specifies only what your final results should be. Follow the approach of splitting the complete design problem into stages, and proceed only when a simpler block performs as expected. You need to organize and conduct the necessary experiments on your own. For example, before testing data transmission through one of the channels, it is a good idea to test first that the system works for a steady logic level 1 or a steady logic level 0. With a dc input, it is easy to verify voltage levels, frequencies, whether the PLL is locked or not, etc.

In the report, you are expected to describe your theoretical and experimental work in detail. Justify all configurations and component selections. Justify each experimental setup and describe the obtained results. Describe any design iterations (errors and error corrections) you made along the way. Finally, your lab work and the report should include the following:

1. Design and demonstrate operation of the channel A: you should build and test the transmitter in the modem 1 and the receiver in the modem 2 of Fig. 1. Channel A should operate according to the design specifications. The data source T_x can be a square-wave signal coming from a pulse generator. In this part, point 1 of the receiver is tied to the ground (test).

To test the transmission at 500bps, set the pulse generator frequency at $f_s = 250\text{Hz}$, duty ratio $D = 0.5$. This test corresponds to the periodic data sequence $\dots 0101010101\dots$, at the 500bps baud rate. The modem works according to the specifications *only* if the received signal is the same as the transmitted signal. Get a hardcopy, or sketch waveforms T_x , v_{osct} , v_{line} , v_{ir} , v_{or} , R_x . Use T_x as the reference and trigger waveform for all other waveforms. Include a hardcopy of T_x and R_x from the same scope screen. R_x is error-free if the corresponding logic levels are the same as in T_x , and if it has no extra transitions. Any glitches in R_x are considered errors.

2. Attempt to increase the baud rate. Find the maximum baud-rate for the error-free channel-A transmission, using the same test sequence as in part (1). To increase the baud rate, you may need to change the filter configuration in the PLL, or between the PLL and the comparator. For the maximum B_r you can achieve, report the same waveforms as in part (1).
3. Repeat parts (1) and (2) for the channel B. Before you redesign the transmitter and the receiver for channel-B operation, make sure that you have a final copy of the complete circuit diagram and design for channel A.
4. Combine the results of channel-A, and channel-B design to make a circuit of a complete modem 1 (or a complete modem 2). *You will need to make just one complete modem.* Verify full-duplex operation with another group of students. One group should make modem 1, the other should make modem 2. Only one pair of wires (one signal and one ground) is allowed to link the two modems. Operate your transmitter at the nominal baud-rate $B_r = 500\text{bps}$, and attempt to demodulate the other group's signal at the same baud rate. Do the test as in part (1). Indicate in the report the group this experiment was performed with, and describe the results. Include a set of your transmitter waveforms, T_x , v_{osct} , v_{line} , referenced to T_x , and a separate set of receiver waveforms, v_{line} , v_{ir} , v_{or} and R_x , referenced to R_x . Your transmitter waveforms will serve as a reference to evaluate the other group's receiver performance. Your receiver waveforms will be compared against the other group's transmitter waveforms. The purpose is to show that your receiver successfully demodulates the other group's transmitted signal.

4.1 Connecting two PC-s through the FSK modems

Connect two PCs through the modems, using T_x (output) and R_x (input) on the PC's serial ports. Serial-port cables are available in the lab. Serial-port communication is governed by the standard known as RS-232, which specifies data formats, timing waveforms, baud rates, voltage and impedance levels etc. This is a part of the RS-232 standard that you must observe when you connect the the serial-port input R_x and output T_x to your modem:

1. An RS-232 output must generate voltage levels of +5V to +15V (representing logic low) and -5V to -15V (representing logic high) into a load of $3k\Omega$ to $7k\Omega$.

2. An RS-232 input must present a load of $3k\Omega$ to $7k\Omega$, converting an input of $+3V$ to $+25V$ to logic low, and an input of $-3V$ to $-25V$ to logic high.

In the RS-232 standard, logic high is represented by a negative voltage level called “mark”, while logic low is represented by a positive voltage level called “space”.

In your report, include schematics of the circuits you used to confirm with the RS-232 standard at the input and the output of your modem. **Check your design with the instructor in the lab before connecting the modem to a PC.**

In the report, specify the baud rate at which you operated the connection between two PCs.

4.2 A simple free-space optical link

A simple free-space optical link can be designed using a light-emitting diode (LED) as opto-transmitter and a photo-transistor (PT) as opto-receiver. Design a circuit to drive the LED from the modem transmitter output and a circuit to connect the photo-transistor to the modem receiver input. It is desired to operate the optical link with at least 1 inch space between the LED and the PT. In your report, include the complete, labeled circuit diagrams of the additional circuits, and hard copies of the waveforms illustrating operation of the optical link. Report the baud rate and the LED/PT distance at which you operated the optical link.

5 Prelab Assignment

The prelab assignment is due in the lab on the day when you start working on the experiment.

Read the complete Lab 5 handout.

Draw a complete labeled circuit diagram with all component values selected for the channel A of the system shown in Fig. 1: the transmitter A in the modem 1, and the receiver A in the modem 2. As given in Section 2, channel A operates with $f_{LA} = 9.5kHz$, $f_{HA} = 10.5kHz$. Assume that the data is transmitted from modem 1 to modem 2 only.

Make a copy of your prelab work so that you can use it during the Lab session.