

## Experiment #6 A/D Converter Design

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In this lab assignment your task is to design an A/D converter using general-purpose integrated and discrete components according to the following specifications:

1. Analog input voltage range is  $0 \leq V_i < 10\text{V}$  (the full-scale voltage is 10V).
2. The outputs are TTL logic levels.
3. The available supply voltages are +15V, -15V, and +5V
4. The active components available for the design are:
  - (a) Integrated and discrete active components used in Labs #1-#5, including D/A converter DAC0808.
  - (b) Logic gates, counters, etc. from the TTL or CMOS 74XXX series.

Instead of the A/D converter design, you can also choose to work on a design project of your choice. Consult with the instructors about your project topic.

This handout gives an introduction to A/D converter characteristics, testing, and A/D converter types. Characteristics common to all types of A/D converters are discussed in Section 1, together with a test circuit that can be used to verify A/D converter performance. Operating principles and block diagrams of several popular types of A/D converters are described in Section 2. Laboratory tasks are outlined in Section 3. The prelab assignment is in Section 4.

### 1 A/D Converter Characteristics and Testing

Analog-to-digital (A/D) converter is a device that for a given analog input voltage  $V_i$  produces an  $n$ -bit digital word at the output. Ideal static characteristics of an A/D converter with unipolar input voltage range,  $0 \leq V_i < V_{ref}$  are shown in Fig. 1. The range of analog input voltages is bounded from above by the *full-scale voltage*  $V_{ref}$ . The number of bits  $n$  in the output is called the *resolution* of the A/D converter. We assume that the output is in the unsigned binary format

$$Output = \{a_1, a_2, \dots, a_n\},$$

where  $a_k = \{0, 1\}$ ,  $a_1$  is the *most significant bit* (MSB), and  $a_n$  is the *least significant bit* (LSB). Given the  $n$ -bit binary output word, the decimal equivalent  $N$  can be found as

$$N = \sum_{k=1}^n a_k 2^{(n-k)} \quad (1)$$

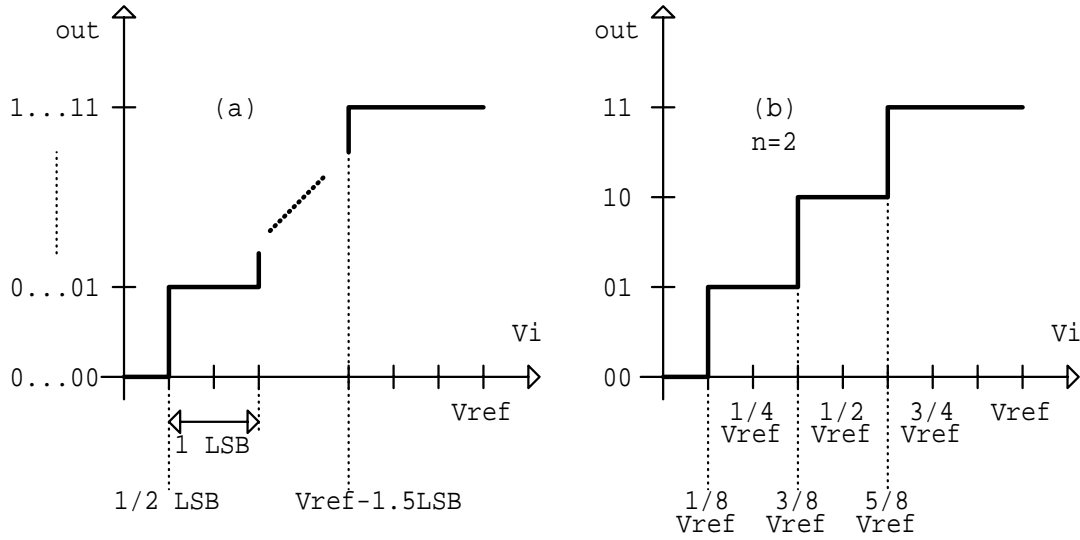


Figure 1: Ideal static characteristic of a unipolar A/D converter with full-scale voltage  $V_{ref}$  for: (a) the general case with resolution  $n$ ; (b) the  $n = 2$  example.

Analog equivalent of the least significant bit is

$$1\text{LSB} = \frac{V_{ref}}{2^n} \quad (2)$$

Given an analog input  $V_i$ ,  $0 \leq V_i < V_{ref}$ , the ideal conversion characteristics shown in Fig. 1 can be written as

$$N = \left[ 2^n \frac{V_i}{V_{ref}} \right] \quad (3)$$

where  $N$  is the decimal integer equivalent of the binary output word, and the brackets  $[\cdot]$  indicate that the result is *rounded* to the nearest integer.

The time it takes to perform a conversion is called the *conversion time*  $T_c$ . Generic timing waveforms for an A/D converter are shown in Fig. 2. A low-to-high transition of the start-of-conversion input signal SOC resets the converter internal circuitry and initiates the conversion. Valid output is available upon low-to-high transition of the *end-of-conversion* EOC output signal. In a general-purpose A/D converter signals SOC and EOC (or their equivalents) are available to facilitate interface between the A/D converter and the digital part of the system (such as a microcontroller that reads the data from the A/D converter). In the Lab, you will design the A/D control circuitry so that a new conversion is started automatically after the previous conversion has been completed. Thus, the digital outputs should be updated periodically at the sampling rate  $f_s$  close to  $1/T_c$ . This mode of A/D operation, where no external signals are necessary to initiate the conversion, is called the *free-running mode*.

The resolution  $n$  and the sampling rate  $f_s$  are the two main characteristics of any A/D converter.

Once you complete the A/D circuit design, the actual static and dynamic characteristics can be tested using the setup shown in Fig. 3. The outputs of the A/D converter under test are connected to the  $n$  most

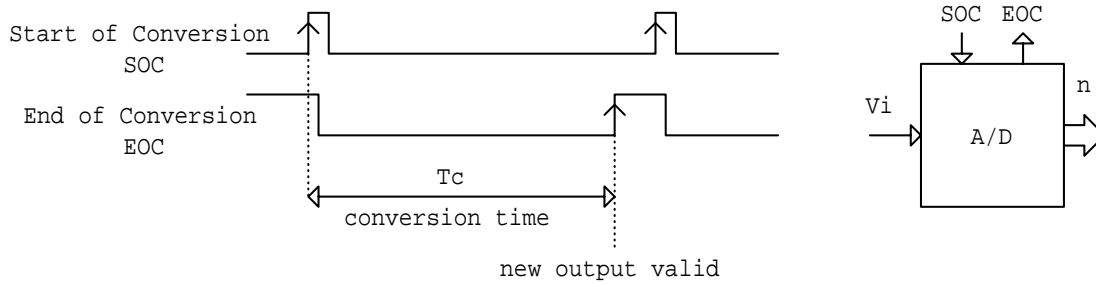


Figure 2: In an A/D converter, an external signal Start-of-Conversion is used to reset the internal circuitry and initiate the conversion. After the conversion period  $T_c$ , the End-of-Conversion signals valid output data.

significant inputs of a D/A converter of higher resolution  $n_{da} > n$ . The D/A resolution should be such that any errors in the output can be attributed to the A/D converter. Both converters are operated with the same reference voltage. Give the decimal equivalent  $N$  at the D/A input, the D/A output is ideally given by

$$V_{da} = \frac{N}{2^n} V_{ref} \quad (4)$$

The test setup output  $V_e$  is obtained by subtracting the input  $V_i$  from the D/A output,

$$V_e = V_{da} - V_i \quad (5)$$

For an ideal A/D converter the output,

$$V_e = \frac{N}{2^n} V_{ref} - V_i = \frac{1}{2^n} \left[ 2^n \frac{V_i}{V_{ref}} \right] - V_{ref} \quad (6)$$

is shown in Fig. 3 as a function of  $V_i$ . The output  $V_e$  is in fact the *quantization error* of the A/D converter.

The complete test circuit using the DAC0808 D/A converter (which was used in Lab 2) is shown in Fig. 4. This is an 8-bit D/A converter, so that the A/D converter under test should have  $n < 8$ . In practice, the tests with  $n = 8$  still produce reasonable results, but if you attempt to construct an A/D converter with  $n > 8$  (this would be a difficult task) a higher-resolution D/A converter should be used. The output op-amp LF356 is used to sum the D/A output current and the current proportional to  $V_i$  (through  $R_2$ ). To obtain  $V_e$ , it is important that  $R_1$  and  $R_2$  are exactly the same if the reference current  $I_{ref}$  for the D/A converter is obtained from the full-scale reference  $V_{ref}$  used in the A/D converter.

In the test circuit, a variable DC input  $V_i$  can be used to test the static A/D conversion characteristic. In addition, a sufficiently slow triangle-wave  $V_i(t)$  can be used to scan all values of  $V_i$  between 0 and  $V_{ref} - 1LSB$ . With the triangle-wave input, the scope screen should look like the waveform in Fig. 3 and any additional errors in the A/D conversion function can be easily observed.

## 2 A/D Converter Types

A/D converters can be classified based on the conversion method as:

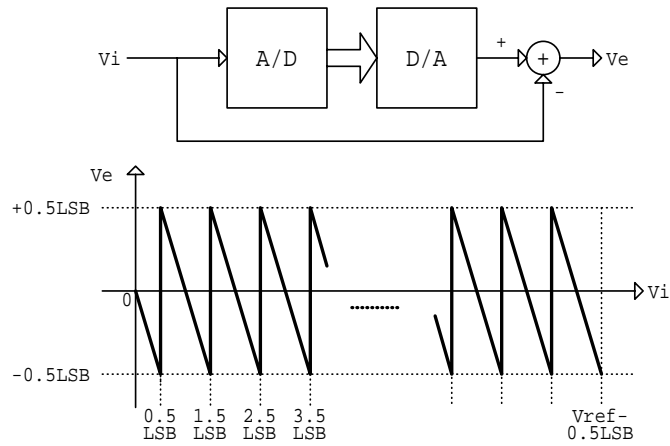


Figure 3: Block diagram of the A/D converter test circuit, and the error voltage output  $V_e$  as a function of the analog input voltage  $V_i$  for an ideal A/D converter.  $1\text{LSB} = V_{ref}/2^n$ .

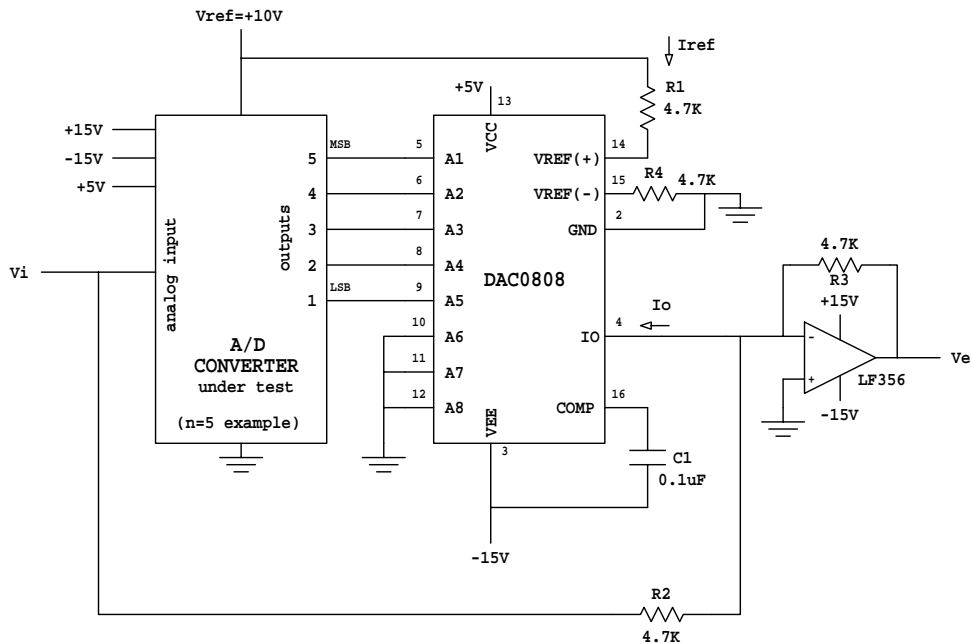


Figure 4: A/D converter test circuit using the DAC0800 D/A converter. The circuit is shown for the  $n = 5$  example.

1. Integrating A/D Converters
  - (a) Voltage-to-frequency
  - (b) Single-slope
  - (c) Charge-balancing, delta-sigma
  - (d) Dual-slope
2. Counting A/D Converters
  - (a) Counter-ramp
  - (b) Tracking
3. Successive Approximation A/D Converters
  - (a) Successive approximation
  - (b) Algorithmic
4. Parallel (Flash) A/D Converters
  - (a) Single-step
  - (b) Multiple-step

In this list, in general, the achievable resolution  $n$  decreases and the achievable sampling rate  $f_s$  increases from top to bottom. Various A/D converter types find different applications depending on the resolution/sampling rate requirements. For example, dual-slope integrating A/D converters are commonly found in digital multimeters where high resolution (20 bits or more) is required but the sampling rate is relatively low. In contrast, parallel (flash) converters with relatively low resolution (8 bits) and high sampling rate (GHz) are used in front ends of high-speed digital oscilloscopes. Successive-approximation converters are the most popular general-purpose A/D converters for medium-resolution (8-16 bits), medium-speed applications.

This section summarizes operating principles and characteristics of several popular types of A/D converters. You are welcome and encouraged to work on other types or variations not described in this handout. You may get extra credit for original, well documented designs.

## 2.1 Voltage-to-Frequency A/D Converter

One of the simplest A/D technique is based on converting the input analog voltage  $V_i$  to frequency, and then to measure the frequency by counting the number of pulses generated during a fixed time interval. A block diagram of the voltage-to-frequency A/D converter is shown in Fig. 5. Analog input  $V_i$  is the input voltage to the voltage-controlled oscillator (VCO) constructed using an integrator with reset, and a voltage comparator COMP. A similar VCO circuit was designed and tested in Lab 3. An  $n$ -bit binary counter with reset R and clock CLK inputs is used to count the number of pulses CK generated by the VCO during a fixed time interval determined by the external clock C. An  $n$ -bit latch with write W input is used to store the valid result of conversion. For the purpose of discussing operation of the converter illustrated by the typical waveforms of Fig. 6, all inputs to the counter and the latch are assumed to be rising-edge triggered. The actual waveform details may be different depending on the choice of components used to implement the converter.

At the beginning of a conversion period, high-to-low transition of the clock C initiates reset of the  $n$ -bit binary counter. During the time  $0 \leq t \leq t_1$  when the switch  $S$  is off, the input voltage  $V_i$  is integrated,

$$V_{int}(t) = \frac{1}{RC} \int_0^t V_i(\tau) d\tau. \quad (7)$$

If the input voltage is constant,  $V_i(t) = V_i = \text{const.}$ , the integrator output is a linear function of time, with the slope proportional to the input  $V_i$ ,

$$V_{int}(t) = \frac{V_i}{RC} t. \quad (8)$$

At  $t = t_1$ ,  $V_{int}(t_1) = V_{ref}$ , and the comparator output CP goes high. As a result, a short pulse CK is generated to reset the integrator back to zero and to increase the binary count by one. In the control logic block, a monostable circuit can be used to generate the short clock pulse CK when triggered by the comparator output CP. The pulse period is

$$t_1 = \frac{V_{ref}}{V_i} RC. \quad (9)$$

During the conversion time  $T_c$ , which is set by the period of the external clock C, the number  $N$  of generated pulses is:

$$N \approx \frac{T_c}{t_1} = \frac{T_c}{RC} \frac{V_i}{V_{ref}} \quad (10)$$

assuming that the length of the clock pulse CK is relatively small compared to  $t_1$ . If  $T_c$  and  $RC$  are selected so that  $T_c = 2^n RC$ , the count  $N$  represents the ideal A/D output,

$$N = \left\lceil 2^n \frac{V_i}{V_{ref}} \right\rceil. \quad (11)$$

At the end of the conversion period, the falling edge of the clock C is used to generate a write W pulse to latch the counter output, and *after that* to generate the pulse R which resets the counter back to all zeros. The circuit is ready for the next conversion.

The conversion period for an  $n$ -bit voltage-to-frequency A/D is approximately  $2^n (t_1)_{min}$ , where  $(t_1)_{min}$  corresponds to the maximum  $V_i$  and maximum frequency of CK pulses. The accuracy and speed are limited by the requirement that the length  $t_{CK}$  of CK is much smaller than  $(t_1)_{min}$ . The CK pulse must be long enough to reset the capacitor  $C$  to zero by turning the switch  $S$  on. This, in turn puts a lower limit on  $(t_1)_{min} \approx RC$ . Since the conversion period equals to approximately  $2^n RC$ , the sampling rate of the voltage-to-frequency A/D is very low, and decreases with increasing the resolution  $n$ . If, for example, it takes about  $t_{CK} = 500\text{ns}$  to reset the capacitor to zero, and the desired resolution is  $n = 8$  bits, the error of less than 0.5LSB can be obtained if we choose  $(t_1)_{min} = RC = 2^{n+1} t_{CK}$ . The total conversion time is  $2^n RC = 2^{2n+1} t_{CK} = 66\text{ms}$ , which corresponds to the sampling rate of only 15Hz. Another factor limiting accuracy of the voltage-to-frequency A/D is the requirement that the external clock period  $T_c$  and the integrator time constant  $RC$  have an exact ratio of  $2^n$ . Any variations in  $R$ ,  $C$  or  $T_c$  proportionally result in gain errors of the A/D converter.

## 2.2 Single-Slope Integrating A/D Converter

Another simple A/D technique is to convert the input analog voltage to time, and then to measure the time by counting the number of fixed-frequency pulses. A block diagram of the voltage-to-time A/D converter also

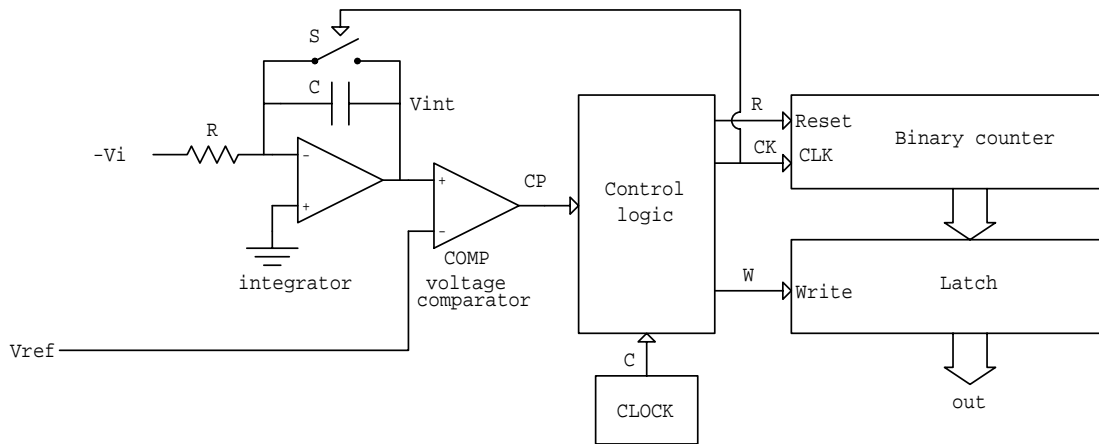


Figure 5: A block diagram of the voltage-to-frequency A/D converter.

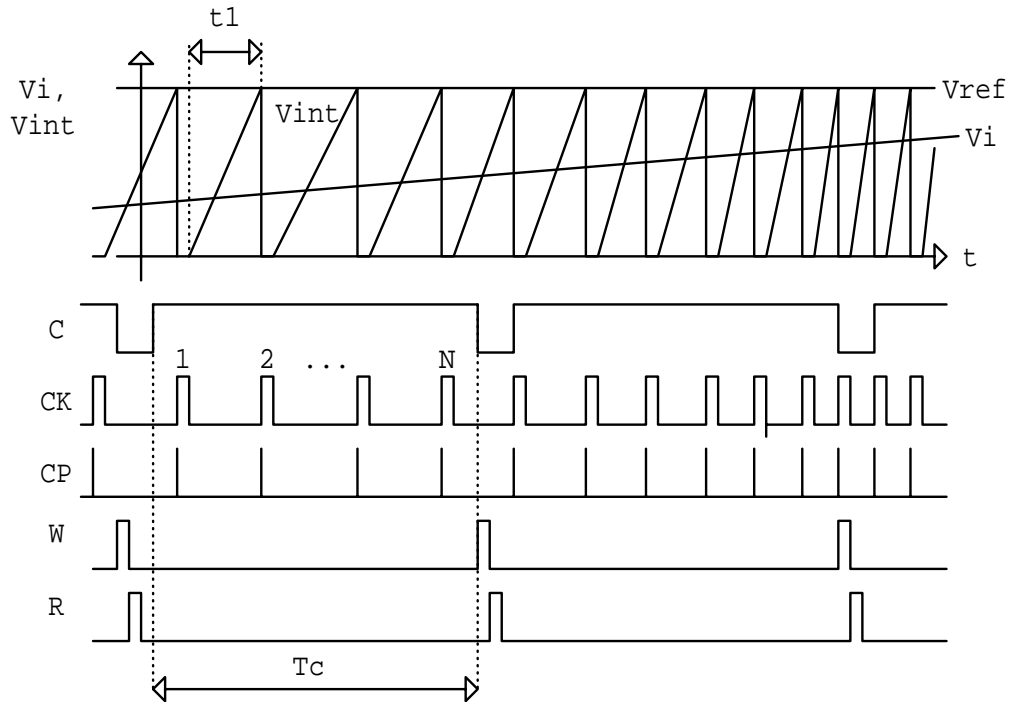


Figure 6: Typical waveforms in the voltage-to-frequency A/D converter.

called the single-slope integrating A/D converter is shown in Fig. 7. Analog input  $V_i$  is the input voltage to the comparator COMP, while the reference  $-V_{ref}$  is integrated to generate the ramp signal  $V_{int}(t)$ . A similar circuit was designed and tested in Lab 2. An  $n$ -bit binary counter with reset R and clock CLK inputs is used to count the number of fixed-frequency pulses CK generated by an external clock during the time interval  $T_c$  until the ramp  $V_{int}(t)$  reaches the analog input  $V_i$ . An  $n$ -bit latch with write W input is used to store the counter output as the conversion result. For the purpose of discussing operation of the converter, illustrated by the typical waveforms of Fig. 8, all inputs to the counter and the latch are assumed to be rising-edge triggered. The actual waveform details may be different depending on the choice of components used to implement the converter.

At the beginning of a conversion period, the  $n$ -bit binary counter and the integrator are reset by the signal R. When R goes low, the switch  $S$  is turned off and the fixed-frequency clock pulses CK are passed to the clock input of the binary counter. The integrator output is

$$V_{int}(t) = \frac{V_{ref}}{RC} t \quad (12)$$

At the end of the conversion period,  $V_{int}(T_c) = V_i$ , the comparator output CP goes high, which ends the conversion:

$$T_c = \frac{V_i}{V_{ref}} RC. \quad (13)$$

If  $T$  is the clock period, during the time  $T_c$  the counter counts up  $N$  pulses,

$$N \approx \frac{T_c}{T} = \frac{RC}{T} \frac{V_i}{V_{ref}} \quad (14)$$

If  $T$  and  $RC$  are selected so that  $RC = 2^n T$ , the count  $N$  represents the ideal A/D output,

$$N = \left\lceil 2^n \frac{V_i}{V_{ref}} \right\rceil. \quad (15)$$

At the end of the conversion period, the rising edge of the comparator output CP is used to generate a write W pulse to latch the counter output, and *after that* the pulse R to reset the counter back to all zeros. The circuit is ready for next conversion.

For an  $n$ -bit conversion, the conversion time goes up to  $2^n T$ , where  $T$  is the period of the external clock used to measure the time  $T_c$ . This limits the achievable sampling rate of the single-slope A/D converter. If, for example, the clock frequency is 1MHz,  $T = 1\mu s$ , and  $n = 8$  is required, the conversion time is up to about  $256\mu s$ , which limits the sampling rate to about 3.9kHz. The main factor limiting accuracy of the voltage-to-frequency A/D is the requirement that the integrator time constant  $RC$  and the external clock period  $T$  have an exact ratio of  $2^n$ . Any variations in  $R$ ,  $C$  or  $T$  proportionally result in gain errors of the A/D converter.

### 2.3 Dual-Slope Integrating A/D Converter

A block-diagram of the dual-slope integrating A/D converter is shown in Fig. 9. This converter is based on the same principle as the single-slope converter of Section 2.2: convert the analog input to time, and then measure the time by counting fixed-frequency pulses. The improvement over the single-slope converter comes from using *the same* integrator to integrate first the input voltage  $V_i$  and then the reference  $-V_{ref}$ .

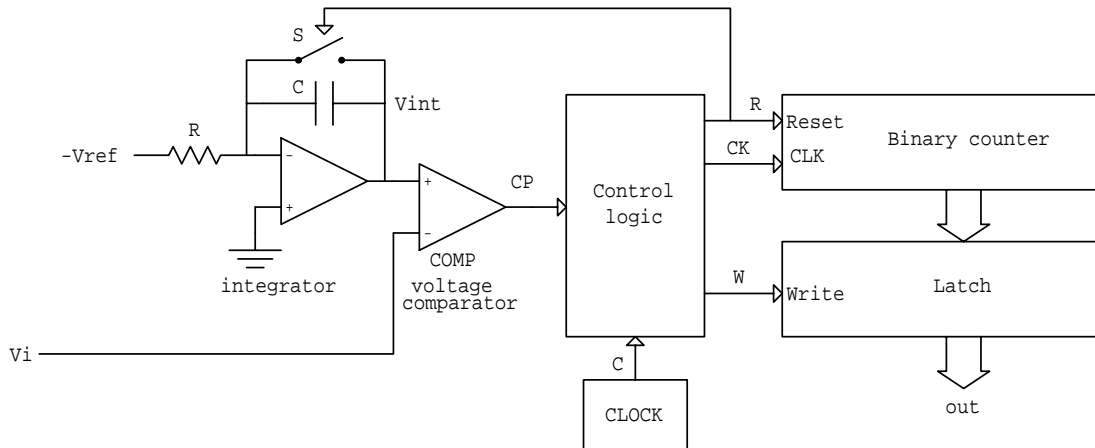


Figure 7: A block diagram of the single-slope integrating A/D converter.

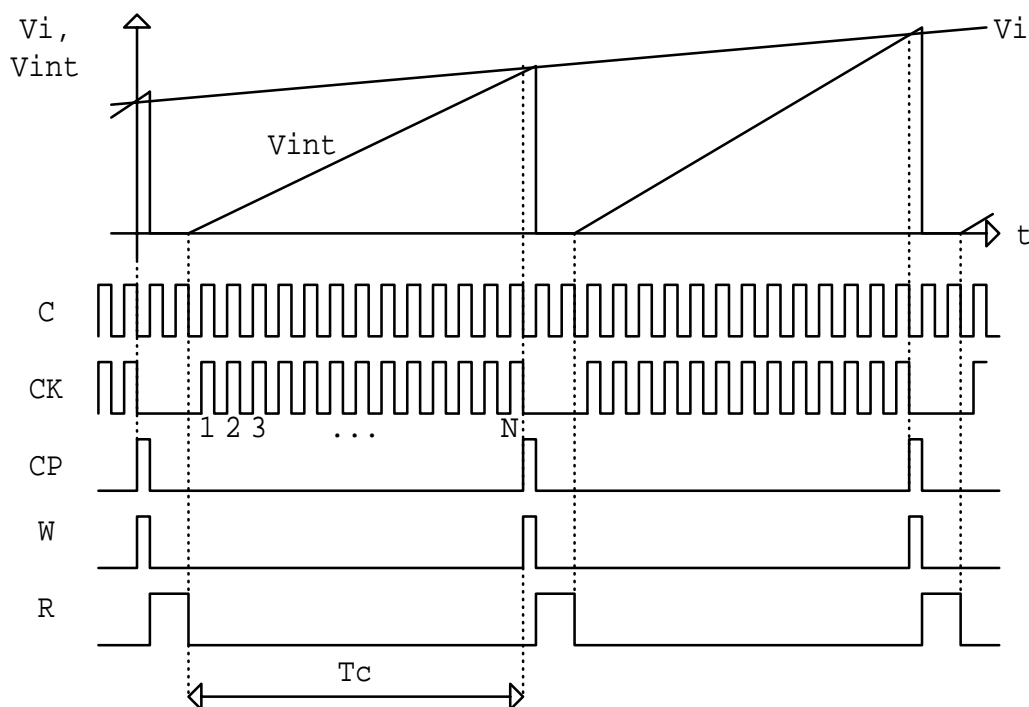


Figure 8: Typical waveforms in the single-slope integrating A/D converter.

As a result, the conversion function of the dual-slope converter does not depend on exact values of the time-constant  $RC$  or the clock period  $T$ .

As shown in Fig. 9, the integrator is built using  $R$ ,  $C$  and a switch  $S$  around an op-amp. A similar circuit was designed and tested in Lab 2. Switches  $S_1$ ,  $S_2$  are used to bring either the input  $V_i$  or the reference  $-V_{ref}$  to the input of the integrator. Zero crossing of the integrator output  $V_{int}$  is detected using the voltage comparator COMP. An  $(n + 1)$ -bit binary counter with reset R and clock CLK inputs is used to count the number of fixed-frequency pulses CK generated by an external clock during the conversion period. The most significant  $(n + 1)^{th}$  bit of the counter is used as the signal Q to control the switches  $S_1$  and  $S_2$ . An  $n$ -bit latch with write W input is used to store the counter output as the conversion result. For the purpose of discussing operation of the converter illustrated by the typical waveforms of Fig. 10, all inputs to the counter and the latch are assumed to be rising-edge triggered. The actual waveform details may be different depending on the choice of components used to implement the converter.

At the beginning of a conversion period, the  $(n + 1)$ -bit binary counter and the integrator are reset by the signal R. When R goes low, the switch  $S$  is turned off and the fixed-frequency clock pulses CK are passed to the clock input of the binary counter. The switch  $S_1$  is on and the switch  $S_2$  is off, so that the integrator output, assuming constant  $V_i$ , is

$$V_{int}(t) = -\frac{V_i}{RC}t \quad (16)$$

At the end of the first interval  $t_1$ , the counter counts up through  $2^n$  pulses, and goes from  $011 \cdots 1$  to  $100 \cdots 0$ . The  $(n + 1)^{th}$  bit  $Q$  goes high, the switch  $S_1$  is turned off and the switch  $S_2$  is turned on. The length of the interval  $t_1$  is therefore

$$t_1 = 2^n T \quad (17)$$

so that the integrator output at the end of this interval is

$$V_{int}(t_1) = V_1 = -\frac{V_i}{RC}2^n T \quad (18)$$

In the second interval,  $-V_{ref}$  is integrated using *the same* integrator, so that

$$V_{int}(t) = V_1 + \frac{V_{ref}}{RC}(t - t_1) \quad (19)$$

The conversion ends at the time when the integrator output crosses zero. The length of the second interval  $t_2$  is

$$t_2 = -\frac{V_1}{V_{ref}}RC \quad (20)$$

During the second interval, the counter counts up  $N$  pulses,

$$N \approx \frac{t_2}{T} \quad (21)$$

Combining (17) through (21), the final count  $N$  is given by

$$N = \left[ 2^n \frac{V_i}{V_{ref}} \right], \quad (22)$$

which is the ideal conversion function. The most important point to note here is that **both**  $RC$  and  $T$  cancel out from the final expression for  $N$ , so that accuracy of the converter is not affected by the exact values of  $T$ ,

$R$  or  $C$ . The choice of  $R$ ,  $C$  and  $T$  is still important in a practical implementation because one must make sure that the clock rate is within the limits of the components used in the design, and that voltage variations are also within the component and supply limits.

At the end of the conversion period, the rising edge of the comparator output  $CP$  is used to generate a write  $W$  pulse to latch the counter output, and *after that* the pulse  $R$  to reset the counter and the integrator back to zero. The circuit is then ready for the next conversion.

For an  $n$ -bit conversion, the conversion time goes up to  $2^{n+1}T$ , where  $T$  is the period of the external clock used to measure the times  $t_1$  and  $t_2$ . This limits the achievable sampling rate of the dual-slope A/D converter. If, for example, the clock frequency is 1MHz,  $T = 1\mu s$ , and  $n = 8$  is required, the conversion time is up to about  $512\mu s$ , which limits the sampling rate to about 1.8kHz. The main advantage of the dual-slope converter is that its accuracy is not affected by the accuracy of the clock period  $T$  or the integrator time constant  $R$ ,  $C$ . Another advantage of this converter is that the analog input is integrated in the conversion process. This has the effect of low-pass filtering any noise signal that may be present at the input. Dual-slope A/D converters are frequently used in high-resolution, low-sampling-rate applications such as digital multimeters.

## 2.4 Counter-Ramp A/D Converter

The counter-ramp A/D converter is very similar to the single-slope integrating A/D converter described in Section 2.2. The block diagram in Fig. 11 can be compared to the block diagram of Fig. 7. Instead of using an analog integrator, the ramp signal  $V_{int}(t)$  is generated directly from the binary counter output using a D/A converter. As in the single-slope integrating A/D, the conversion ends when the ramp signal  $V_{int}(t)$  at the  $+$  input of the voltage comparator  $COMP$  reaches the analog input  $V_i$  at the  $-$  input of the comparator. An  $n$ -bit binary counter with reset  $R$  and clock  $CLK$  inputs is used to count the number of fixed-frequency pulses  $CK$  generated by an external clock. An  $n$ -bit latch with write  $W$  input is used to store the conversion result. For the purpose of discussing operation of the converter using the typical waveforms of Fig. 8, all inputs to the counter and the latch are assumed to be rising-edge triggered. The actual waveform details may be different depending on the choice of components used to implement the converter.

At the beginning of a conversion period, the  $n$ -bit binary counter is reset by the signal  $R$ . When  $R$  goes low, the counter counts up the clock pulses  $CK$ , and the D/A output  $V_{int}(t)$  increases in 1LSB steps. At the end of the conversion period,  $V_{int}(T_c) > V_i$ ,

$$V_{int}(T_c) = \frac{N+1}{2^n} V_{ref} > V_i, \quad (23)$$

which implies

$$N = \left\lceil 2^n \frac{V_i}{V_{ref}} \right\rceil, \quad (24)$$

Note that a 0.5LSB offset is added to the D/A output to obtain the ideal A/D conversion characteristic.

At the end of the conversion period, the rising edge of the comparator output  $CP$  is used to generate a write  $W$  pulse to latch the counter output, and *after that* to reset the counter back to all zeros, so that the next conversion period can start.

An advantage of the counter-ramp converter over the single-slope integrating converter is that the ideal conversion function does not depend on the exact value of the clock period  $T$ , and the analog integrator is eliminated so that there is no need for high accuracy of the integrator time constant. As in the single-slope A/D, the sampling rate is limited to about  $1/(2^n T)$  where  $T$  is the clock period. The main limitation for

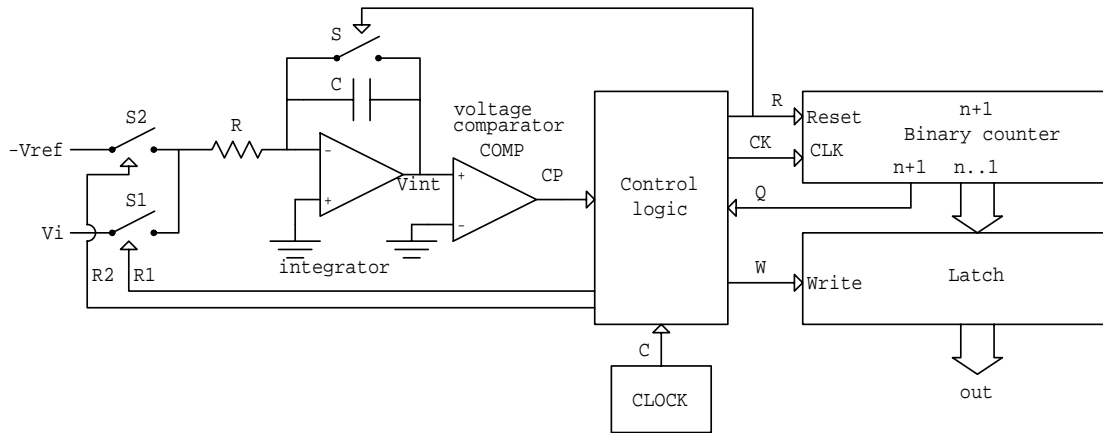


Figure 9: A block diagram of the dual-slope integrating A/D converter.

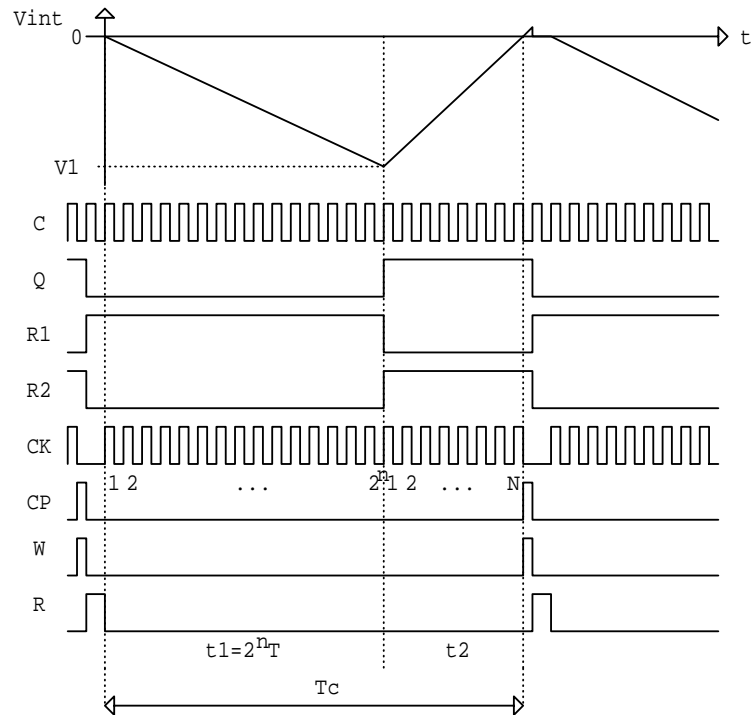


Figure 10: Typical waveforms in the dual-slope integrating A/D converter.

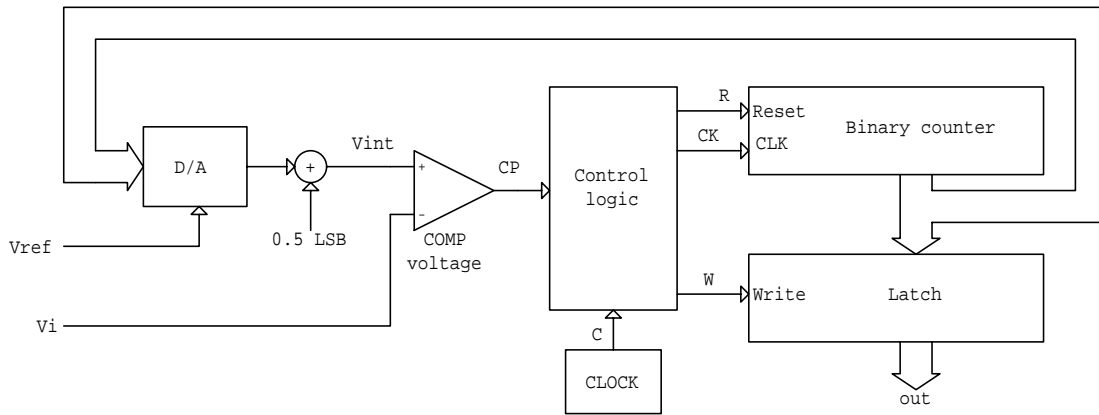


Figure 11: A block diagram of the counter-ramp A/D converter.

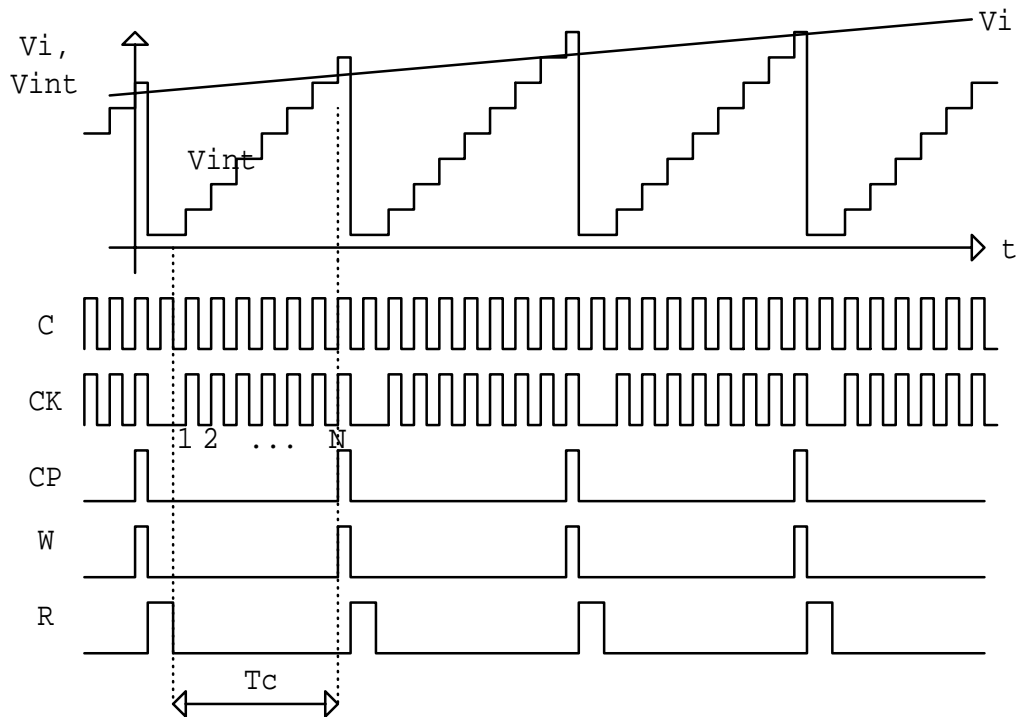


Figure 12: Typical waveforms in the counter-ramp A/D converter.

the clock frequency is the response time of the D/A converter and the comparator. A disadvantage of the counter-ramp converter compared to the dual-slope converter is that the conversion result is affected by the instantaneous value of  $V_i(t)$ , any noise in  $V_i(t)$  is not filtered out, and the noise immunity is lower.

## 2.5 Successive Approximation A/D Converter

The counter-ramp A/D converter of Section 2.4 can be thought of as implementing a linear-search algorithm to find the best possible  $n$ -bit integer approximation to an analog input voltage. A very significant improvement in the sampling rate can be obtained by implementing a much more efficient binary search algorithm. The best approximation is found by testing whether each of the  $n$  bits should be high or low starting from the most significant bit to the least significant bit. The process requires only  $n$  tests as opposed to up to  $2^n$  tests required in the counter-ramp converter.

A block diagram of the successive approximation A/D converter that implements the binary search algorithm is shown in Fig. 13, together with typical waveforms shown in Fig. 14. The block diagram is very similar to the counter-ramp diagram of Fig. 11, except that the binary counter (which implements the linear search) is replaced with a successive-approximation register SAR which implements the binary search. An  $n$ -bit latch with write  $W$  input is used to store the conversion result. For the purpose of discussing operation of the converter using the waveforms of Fig. 14, all inputs to the SAR and the latch are assumed to be rising-edge triggered. The actual waveform details may be different depending on the choice of components used to implement the converter.

In the example waveforms of Fig. 14,  $n = 3$ . At the beginning of a conversion period, SAR is reset by the signal  $R$ . In the first clock period, the most-significant bit of the SAR is set to 1, and the D/A output  $V_{int}$  corresponding to the input 100, offset by 0.5LSB, is compared to the analog input  $V_i$ . If  $V_{int} > V_i$ , the bit is cleared to zero. If  $V_{int} < V_i$ , the bit is retained. The same operation is repeated for the next significant bit until the least significant bit is tested in the  $n^{th}$  clock period. Finally,  $Q$  signals that all  $n$  bits have been tested and that the valid output is available at the SAR output. This is used to generate a write  $W$  pulse to latch the SAR output, and *after that* the pulse  $R$  to reset the SAR. The circuit is ready for the next conversion.

The successive-approximation register can be constructed using an  $(n + 1)$ -bit shift register (to generate the test bits starting from the MSB to the LSB, and the signal  $Q$ ), and another  $n$ -bit latch (memory) to keep the results of voltage comparison, i.e., to keep or to clear the tested bit. In designing the converter, one must pay close attention to the timing waveforms: when the test bit is set, the D/A converter and the comparator take time to respond. After this response time, it is safe to clear or retain the tested bit in the SAR. This limits how high the clock frequency  $1/T$  can be.

The main advantage of the successive-approximation A/D converter is that the conversion period is reduced to only  $n + 1$  clock periods (assuming that it takes 1 clock period to reset and prepare the circuit for the next conversion). If, for example, the clock frequency is 1MHz,  $T = 1\mu s$ , and  $n = 8$  bit resolution is required, the sampling rate is about  $1/((n + 1)T) = 110\text{kHz}$ , much higher than any of the integrating or counter-ramp A/D converters. The instantaneous input  $V_i(t)$  affects the result, and the converter is sensitive to noise. To ensure that  $V_i$  is constant during the conversion period, the successive-approximation converter is usually preceded by a sample-and-hold (S/H) circuit. A sample-and-hold circuit is described in Section 2.6, in relation to parallel (flash) A/D converters.

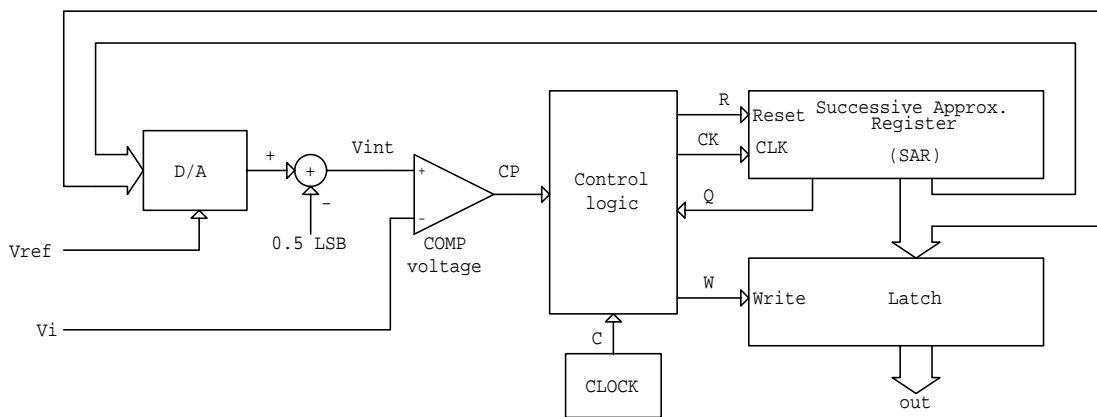


Figure 13: A block diagram of the successive approximation A/D converter.

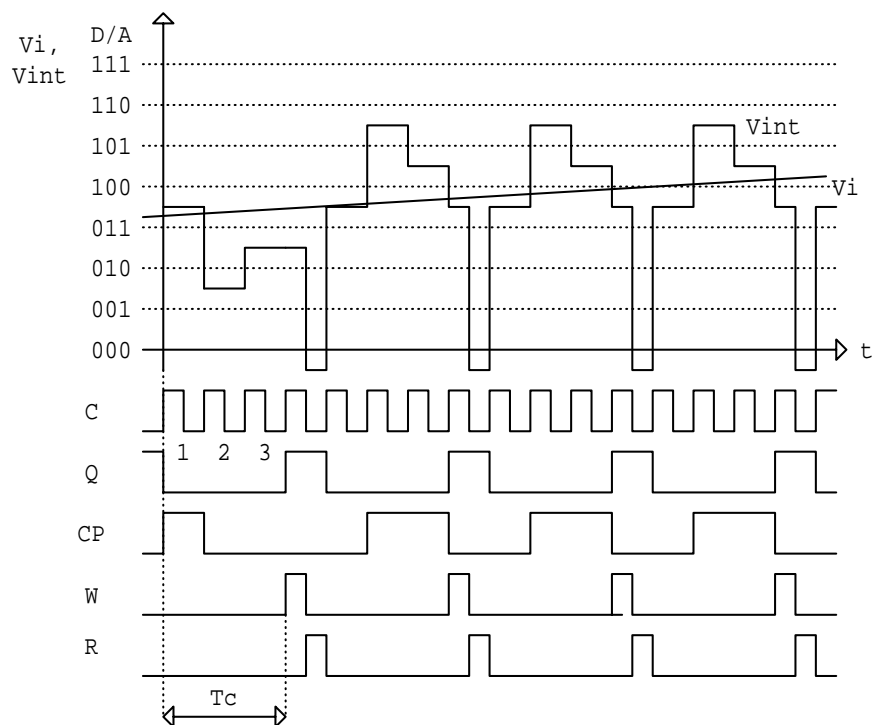


Figure 14: Typical waveforms in the successive approximation A/D converter, assuming  $n = 3$ .

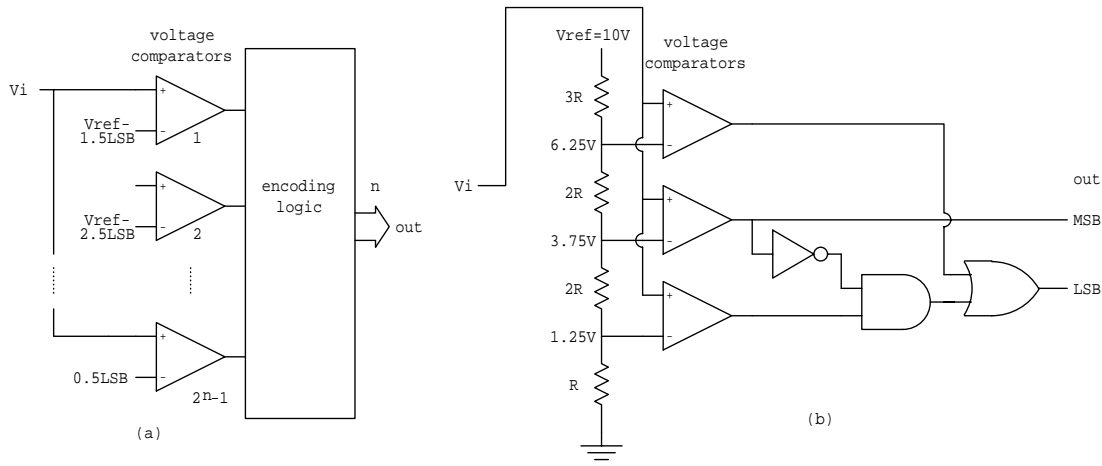


Figure 15: A block diagram of the one-step parallel (flash) converter for: (a) general,  $n$ -bit resolution; (b)  $n = 2$ .

## 2.6 Parallel (Flash) A/D Converters

The basic parallel (flash) A/D converter is shown in Fig. 15. The digital output is obtained by comparing the analog input  $V_i$  simultaneously with a set of voltage references equal to the transition points in the ideal A/D converter characteristic shown in Fig. 1. As shown in Fig. 15(a),  $2^n - 1$  voltage comparators are required to implement an  $n$ -bit flash A/D converter. The  $2^n - 1$  logic-levels at the comparator outputs are then converted to the  $n$ -bit binary output using an encoding logic block. Fig. 15(b) shows how the reference voltages are obtained from  $V_{ref}$  using a resistive voltage divider, and how the encoding logic is implemented using standard logic gates, for the  $n = 2$  example.

The most notable feature of the basic flash converter is that the digital outputs are all obtained almost instantaneously, within the comparator response times and the delays in the encoding logic. Implementation of the basic single-step flash converter is very simple, so that this converter type is specifically *excluded* from your list of choices for the lab experiment. However, the single-step flash converter has a number of interesting extensions that you may consider. One extension, the two-step flash converter is discussed next, while other possible extensions are mentioned at the end of this section.

Fig. 16 shows block diagram of a two-step flash converter, where two  $m$ -bit single-step flash converters are combined to obtain an  $(n = 2m)$ -bit output. The total number of comparators required is  $2^{n/2+1} - 2$ , compared to  $2^n - 1$  in the single-step flash. The first  $m$ -bit flash is used to obtain the  $m$  most-significant bits of the output. An analog equivalent of these  $m$  bits is obtained using an  $m$ -bit D/A converter and is subtracted from the input  $V_i$ . The residual error (up to  $1/2^m$  of  $V_{ref}$ ), amplified by  $2^m$ , feeds the second  $m$ -bit flash A/D used to obtain the  $m$  least significant bits of the output. Because of response times and propagation delays, the output bits are not valid simultaneously. Additional circuitry consisting of a sample-and-hold S/H, clock, and a latch is used to control the conversion and ensure that all valid output bits are available simultaneously at the output. The basic sample-and-hold circuit is shown in Fig. 17, with the typical waveforms shown in Fig. 18. During the clock C low period, the sample-and-hold is in the hold

state, with the S/H output constant and equal to the analog input  $V_i$  sampled at the falling edge of C. During this time, the outputs of the flash converters can settle to the valid steady-state since the analog input is constant. The rising edge of C is used to write the outputs to the latch and the S/H is turned into the `sample` state, when the new value of the analog input  $V_i$  is acquired. Since the conversion is completed within 1 clock period, the two-step flash can have the highest sampling rate out of all A/D converters described in this handout. However, because of the amount of hardware required, it is difficult to obtain the same resolution as in the other types of A/D converters.

The two-step flash concept can be extended to multi-step flash with different ratios of  $m$  and  $n$ . Ultimately, one can construct an  $n$ -step flash with  $m = 1$  bit conversion in each stage. Another interesting variation is to use the same  $m$ -bit flash to obtain both the  $m$  most and the  $m$  least significant bits: after the  $m$  most significant bits are obtained, the amplified error of the first conversion is fed back to the same flash converter to generate the  $m$  least significant bits. This would typically require two clock periods to complete the conversion but significantly reduce the amount of hardware required for implementation. Further extensions of this concept are multi-step schemes known as *algorithmic* A/D converters with various ratios of  $m$  and  $n$ .

### 3 Experiment

In the lab, your task is to design and build a selected A/D converter circuit, verify the actual performance (resolution, sampling rate), demonstrate the working circuit to the instructors during the last lab session, and prepare a detailed report according the same guidelines as in the Labs 1-5. In addition, your report should include:

- A detailed, labeled circuit diagram of the designed A/D converter
- A detailed description of the circuit operation, supported by labeled sketches of timing waveforms and experimental waveforms that illustrate operation of the converter
- Results of testing the converter as described in Section 1
- A discussion of errors observed and possible corrections.

### 4 Prelab Assignment

Your prelab task is to select an A/D converter type, estimate the achievable resolution and sampling rate, and design the converter on paper. Turn in a circuit diagram of your preliminary design.

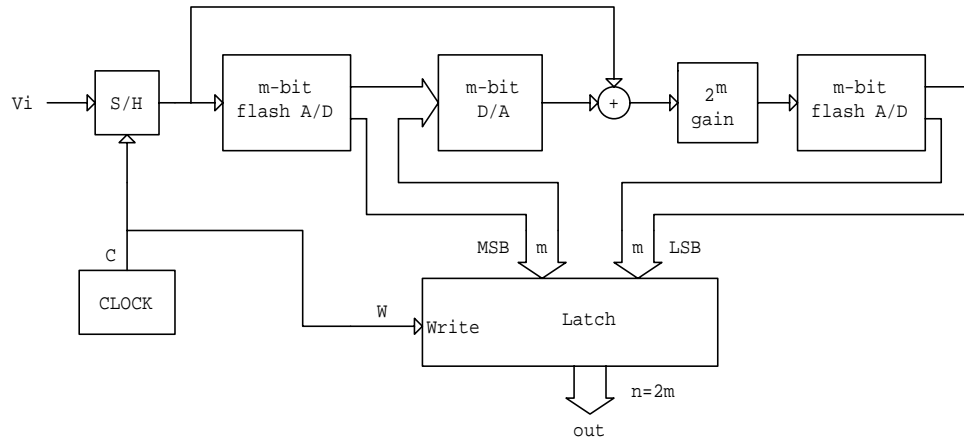


Figure 16: A block diagram of the two-step parallel (flash) converter.

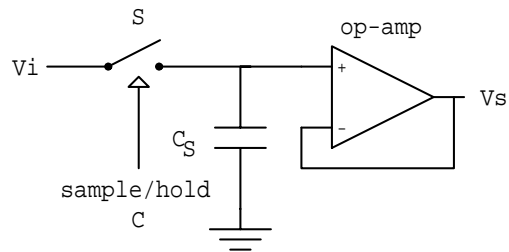


Figure 17: A sample-and-hold circuit.

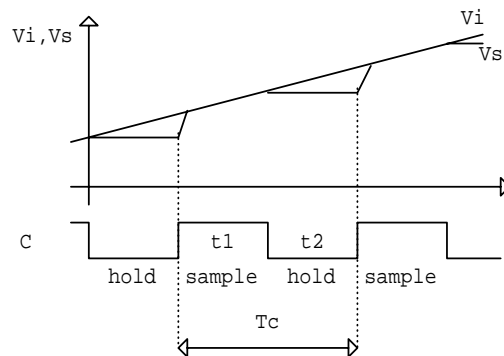


Figure 18: Timing waveforms in the two-step flash A/D converter.