Problem S11. Design of a high-gain, wide-bandwidth amplifier

Design an amplifier in the 0.35u CMOS process having a low frequency gain of at least 40 dB, ability to output an undistorted sinusoidal signal of 1 V peak-to-peak amplitude at 100 kHz, and as high as possible bandwidth $f_{BW}$. A starting point in your design can be the common source amplifier with active load from Problem S.10. The design constraints are as follows:

a. You can use as many NMOS or PMOS transistors as you wish. Note that the body of an NMOS transistor must be tied to the most-negative supply rail (ground in this example), while the body of PMOS transistors can be tied either to the most-positive supply rail ($VDD = 3.3$ V in this example) or to the transistor source. Transistor widths and lengths can be changed as you wish, but only in 1 μm increments (i.e. 1u, 2u, etc.), with an exception of the minimum widths or lengths equal to 0.35 μm, which are also available.

b. A single ideal DC voltage source $VDD = 3.3$ V is available. You are not allowed to change the value of the DC supply voltage $VDD$.

c. A single ideal DC bias current source $IB$ is available. You are allowed to change $IB$ as you wish but only in 1μA increments. At the DC operating point (obtained by .op simulation) there must be no DC voltages outside 0 to $VDD = 3.3$ V range.

d. The input signal voltage source $VIN$ has a DC component, and an ac signal component. You are allowed to adjust the DC component of $VIN$ as you wish in the range from 0 to $VDD = 3.3$ V. The source resistance is $RIN = 47$ kΩ, and you are not allowed to change this value.

e. The output of the amplifier is loaded with $CL = 1pF$ from the output node to ground. You are not allowed to change the value of the capacitance $CL$.

f. You are not allowed to use any other resistors, inductors, capacitors, sources, or active components in your circuit.

g. Bandwidth $f_{BW}$ is the frequency where the magnitude response of $v_{out}/v_{in}$ drops by 3 dB with respect to the low-frequency gain. Any peaking in the magnitude response must be less than 3 dB with respect to the low-frequency gain.

The best design is the one that meets the specs and the constraints, and achieves the widest bandwidth.

Turn in a copy of the LTspice schematic, and simulation results that show undistorted 1 V peak-to-peak sinusoidal voltage at 100 kHz (using .tran simulation), as well as the amplifier’s magnitude response and the value of $f_{BW}$ (using .ac simulation)

**HW policy:** you are allowed to consult with other students taking the class, but copying someone else’s work is not allowed. Students who turn in the same solutions will receive zero credit.

**Extra credit**: students (one ECEN4827 student, one ECEN5827 student) who turn in the best performing amplifiers (widest bandwidth, while meeting all other specs and constraints) will at the end of the semester receive an extra credit that consists of replacing their worst HW score with full credit.