S12 Schmitt trigger logic gate

Figure 1 shows circuit diagram and symbol for a Schmitt trigger logic gate, which exhibits a hysteresis in its input-to-output transfer characteristic. The Schmitt trigger is supplied by $V_{DD} = 3.3$ V. The process is 0.35μ CMOS.

(a) Determine (by hand) the operating regions (triode, saturation or cutoff) of all devices for two cases: $V_{in} = 0$ (logic low), and $V_{in} = V_{DD} = 3.3$ V (logic high).
(b) Using the Schmitt trigger symbol, setup an LTspice simulation to plot the transfer characteristic $V_{out}(V_{in})$ and determine the thresholds $V_H$ and $V_L$. Turn in printouts of the LTspice simulation circuit and its transfer characteristic.
(c) Note that the hysteresis in the transfer characteristic is due to M5 and M6. Find approximate analytical expressions for $V_L$ and $V_H$ in terms of transistor parameters. Compute $V_L$ and $V_H$ based on approximate 0.35μ CMOS device models, and compare the values to the values obtained by simulation in part (b).

Figure 1: Schmitt-trigger circuit, symbol and transfer characteristic