In the CMOS circuit shown in Fig. 1, device parameters are: \((\mu n C_{ox}/2)(W/L) = \mu p C_{ox}/2)(W/L) = K = 25\mu A/V^2\), \(\lambda = 0\), \(\gamma = 0\), \(V_{tn} = -V_{tp} = V_t = 1V\). The supply voltages are \(V_{DD} = 5V\), \(-V_{SS} = -5V\) and the load resistance is \(R = 100k\Omega\). The two input voltages have DC bias components \(V_{I1}, V_{I2}\), and the signal components \(v_{i1}, v_{i2}\).

a) If \(V_{I1} = V_{I2} = 0\), find the DC bias currents \(I_1, I_2, I_3, I_4, I_5, I_6, I_7, I_8\), and the DC bias voltages \(V_{O1}, V_{O2}\), and \(V_O\).

b) At the operating point found in (a), find the signal output \(v_o\) as a function of signal inputs \(v_{i1}\), and \(v_{i2}\).

c) At the operating point found in (a), find the gains \(A_1 = v_{o1}/v_{i1}\) and \(A_2 = v_{o2}/v_{i2}\).

d) Suppose that \(v_{i1} = v_{i2} = 0\), while the DC input voltages can be \(-V_{SS}\) or \(+V_{DD}\). For each combination of the DC input voltages, determine the operating mode (cutoff, triode or active) for all devices, and find the DC output voltage \(V_O\). Put your results in the table:

<table>
<thead>
<tr>
<th>(V_{I1})</th>
<th>(V_{I2})</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
<th>M7</th>
<th>M8</th>
<th>(V_O)</th>
</tr>
</thead>
<tbody>
<tr>
<td>+V_{DD}</td>
<td>+V_{DD}</td>
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<tr>
<td>+V_{DD}</td>
<td>-V_{SS}</td>
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<tr>
<td>-V_{SS}</td>
<td>+V_{DD}</td>
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<tr>
<td>-V_{SS}</td>
<td>-V_{SS}</td>
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</tbody>
</table>

e) Using an additional resistor \(R_1\), and as many devices as you need, construct the DC bias sources \(I_{bias1}\) and \(I_{bias2}\). Sketch your circuit, and find \(R_1\).

![Figure 1:](image-url)