ECEN 4827/5827

Sample Midterm Exam 1
1. [60 pts] In the two-stage CMOS op-amp in Fig. 1(a), the transistor parameters are:

NMOS: $\mu_n C_{ox} = 40 \mu A/V^2$, $V_{th} = 0.7 V$, $\gamma_n = 0$, $\lambda_n = 0.04 \text{ 1/V}$

PMOS: $\mu_p C_{ox} = 20 \mu A/V^2$, $V_{tp} = -0.7 V$, $\gamma_p = 0$, $\lambda_p = 0.04 \text{ 1/V}$

Note that the op-amp has a single supply voltage $V_{DD} = +5 V$.

Figure 1(a)

a) [5 pts] Label the + and – inputs in Figure 1(a).

b) [9 pts] Assuming the DC input and output voltages are $V(+) = V(-) = V_{O1} = V_{DD}/2$, all transistors are in the active/saturation region. Find the DC bias currents $I_{D5}$, $I_{D7}$, $I_{D1}$, and the DC bias voltages $V_{G8}$, $V_{S1}$, and $V_{G6}$. State your approximations.

c) [10 pts] State which transistor(s) determine the limits of the input common-mode voltage range, and find the limits $V_{CMmin}$ and $V_{CMmax}$.

d) [12 pts] At the DC operating point of part (b), find the output resistance $R_{out1}$ and the small-signal open-loop voltage gain $A_1 = V_{o1}/(v(+)−v(-))$. 
e) [6 pts] The op-amp in Figure 1(a) modified as shown in Figure 1(b). Using only MOS transistors, sketch the common-drain output stage.

\[ V_{DD} = +5 \text{ V} \]

\[ v_{O1} \]

\[ v_O \]

\[ v_{OS} \]

\[ I_{DS} \]

\[ I_{B1} \]

\[ I_{B2} \]

\[ I_{B3} \]

\[ M_1 \]

\[ M_2 \]

\[ M_3 \]

\[ M_4 \]

\[ M_5 \]

\[ M_6 \]

\[ M_7 \]

\[ M_8 \]

\[ M_9 \]

\[ M_{10} \]

\[ v_O \]

\[ v_{OS} \]

Figure 1(b)

f) [5 pts] The main purpose of adding the PMOS input stages (\(M_9, M_{10}, I_{B2}\) and \(I_{B3}\)) is to:

1. Improve common-mode rejection ratio
2. Reduce lower limit \(V_{CM_{\text{min}}}\) of the common-mode input voltage range
3. Increase upper limit \(V_{CM_{\text{max}}}\) of the common-mode input voltage range
4. Increase gain
5. Increase output voltage swing

Justify your answer.

g) [5 pts] The main purpose of adding the common-drain output stage is to

1. Improve common-mode rejection ratio
2. Increase output voltage swing
3. Reduce output resistance
4. Reduce input offset voltage
5. Increase gain

Justify your answer.
h) [8 pts] Input offset voltage $V_{OS}$ of the op-amp in Figure 1(b) is found to be $V_{OS} = \pm 10$ mV. When the op-amp in Figure 1(b) is used in the circuit shown in Fig. 1(c), the DC output voltage is $V_O$ with tolerance $\pm \Delta V_O$. Find $V_O$ and $\Delta V_O$ for these two cases:

1. $V_I = -1$ V
2. $V_I = +1$ V

You can assume the resistors $R$ have nominal values with zero tolerances. State any approximations you made.
2. **[40 pts]** Figure 2 shows a realization of the DC current sources $I_{B1}$, $I_{B2}$ and $I_{B3}$ in the op-amp of Figure 1(b). The transistor parameters are:

NMOS: $\mu_n C_{ox} = 40 \mu A/V^2$, $V_{tn} = 0.7 \text{ V}$, $\gamma_n \approx 0$, $\lambda_n = 0.04 \text{ 1/V}$

PMOS: $\mu_p C_{ox} = 20 \mu A/V^2$, $V_{tp} = -0.7 \text{ V}$, $\gamma_p \approx 0$, $\lambda_p = 0.04 \text{ 1/V}$

**Figure 2**

There is no need to sketch the rest of the op-amp in Fig.1(b)

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a) **[10 pts]** Find $R_1$ and $R_b$ so that $I_R = I_B = 1 \mu A$.

b) **[8 pts]** Using only MOS transistors, sketch complete realization of the current sources $I_{B1}$, $I_{B2}$, and $I_{B3}$ in Figure 2. Specify the transistor aspect ratios.

c) **[5 pts]** To minimize the fractional temperature coefficient $TC_T(I_B)$, should $TC_T(R_b)$ be positive or negative? Justify your answer.

d) **[5 pts]** Does the circuit in Fig. 2 require an auxiliary bootstrap circuit to ensure correct start-up? Justify your answer.

e) **[8 pts]** Find (approximately) the sensitivity $S_{V_{DD}}^{I_B}$.

f) **[4 pts]** Suppose that $S_{V_{DD}}^{I_B} = 0.1$ and that $V_{DD}$ increases from $V_{DD} = 5 \text{ V}$ to $V_{DD} = 6 \text{ V}$. How much will $I_B$ increase?