Problem A.40b: two-stage CMOS op-amp

A two-stage CMOS op-amp is shown in Figure 1.

NMOS transistors have: $\mu_n C_{ox} = 50 \text{ }\mu\text{A/V}^2$, $V_{tn} = 0.8 \text{ }\text{V}$, $\gamma \approx 0 \text{ }\text{V}^{1/2}$, $\lambda_n = 0.02 \text{ }\text{V}^{-1}$.

PMOS transistors have: $\mu_p C_{ox} = 20 \text{ }\mu\text{A/V}^2$, $V_{tp} = -0.8 \text{ }\text{V}$, $\gamma \approx 0 \text{ }\text{V}^{1/2}$, $\lambda_p = 0.03 \text{ }\text{V}^{-1}$.

The device aspect ratios $W/L$ (in $\mu\text{m}/\mu\text{m}$) are shown in Figure 1. The supply voltages are $VDD = VSS = 3 \text{ }\text{V}$, and the bias current is $I_B = 5 \text{ }\mu\text{A}$.

![Figure 1: a two-stage CMOS op-amp.](image)

a) The circuit diagram of the op-amp in Figure 1 is not correct: two connecting wires are missing. Add the missing wires in Figure 1.

b) Label + and – inputs of the op-amp.

c) Find $W_7$ for correct op-amp operation with ideally very small input offset voltage.

d) Assuming that $V(+) = V(-) = V_O = 0$, find the device operating regions, all DC drain voltages $V_{Dr}$, and all DC drain currents $I_{Dr}$, $k = 1,\ldots,10$. Put the results in a table.

e) Find the input common-mode voltage range, i.e. the range of input common-mode voltages such that all devices operate in the active/saturation region.

f) Find the output voltage swing of the op-amp, i.e. the range of output voltages such that all devices operate in the active/saturation region.

g) Suppose that $V_{G2} = V_{DD}$, and $V_{G1} = 0$. Find the device operating regions, all DC drain voltages $V_{Dr}$, and all DC drain currents $I_{Dr}$, $k = 1,\ldots,10$. Put the results in a table.

h) At the operating point found in part (d), find the differential-mode open-loop small-signal voltage gain of the op-amp, $A_o = V_o/(v(+) - v(-))$. State the approximations you made.
i) At the operating point found in part (d), find the common-mode open-loop small-signal voltage gain of the op-amp, $A_{cm} = 2 \frac{v_o}{(v(+)+v(-))}$, and the common-mode rejection ratio, CMRR = $A_o / A_{cm}$. State the approximations you made.

j) At the operating point found in part (d), find the open-loop small-signal output resistance $R_{out}$ of the op-amp. State the approximations you made.

k) Using the op-amp of Figure 1, a discrete resistor $R_1 = 10 \, \text{K}\Omega$, and a discrete resistor $R_2 = 100 \, \text{K}\Omega$, sketch a closed-loop amplifier having a closed-loop gain $A_{CL} = \frac{v_o}{v_i}$ of approximately $-10$, $(A_{CL})_{\text{ideal}} = -10)$. Taking into account the results found in parts (h) and (j), find an expression and the value for the actual closed-loop voltage gain $A_{CL}$.