Problem S.8. Op-amp analysis, simulation and output-stage design

Figure 1 shows an op-amp in the 0.35u CMOS process. The op-amp is a “P” version of the standard two-stage configuration discussed in class: a PMOS differential pair M1/M2 is actively loaded by the mirror M3/M4, followed by an NMOS common-source amplifier M6 actively loaded by M7. The role of the Miller compensation capacitor Cc connected between nodes 1 and 2 will be discussed later in class.

Note that the op-amp has a single supply voltage VDD = 3.3 V. It is connected in a unity-gain feedback configuration. The DC input voltage is Vp = 1.65 V.

(a) Using approximate device models for hand calculations, find DC voltages at the nodes b, s, 3, 1, and out, and DC drain currents of all MOS transistors. Compare the results with the operating point (.op) simulation results. Turn in a table with the results.

(b) Assuming the DC bias solution obtained by hand calculations in part (a), find the small-signal open-loop gain $A_o$ of the op-amp at low frequencies. Compare this value to the value obtained by simulation. Describe how you obtained the simulation result for $A_o$.

(c) Add a common-drain (source-follower) stage to the amplifier. Choose bias and aspect ratios of the additional devices so that the small-signal open-loop output resistance of the op-amp (according to approximate hand calculations) becomes $r_{out} = 1 \, k\Omega$. Turn in a copy of the circuit diagram. Describe the simulation setup you used to find the actual $r_{out}$ and report the result you obtained by simulation.