DC Solution in the two-stage CMOS op-amp (part 2)

Our objective is to determine the DC voltage at the Node 1, i.e. the DC voltage at the drain of M2 (which is also the drain of M4, and the gate of M6). In the previous lecture, we found that M1 and M3 are both operating in the active/saturation region. Furthermore, we have that

$$I_{D1} = I_{D3}$$  \hspace{1cm} (1)

Intuitively, we can guess that the following is true,

$$V_{DS1} = V_{DS2}$$
$$V_{SD3} = V_{SD4}$$  \hspace{1cm} (2)

But how do you prove this? Certainly the gate to source voltages of M1 and M2 are the same and $I_{D1}$ must equal $I_{D3}$. Writing the M1, M3 device characteristics for (1), we get

$$\frac{\mu_p C_{ox}}{2} \left( \frac{W}{L} \right)_1 (V_{GS1} - V_{th})^2 = \frac{\mu_p C_{ox}}{2} \left( \frac{W}{L} \right)_3 (V_{SG3} - V_{th})^2$$  \hspace{1cm} (3)

Similarly, since
and assuming that both M2 and M4 in the active/saturation region, we have

\[
\frac{\mu_n C_{ox}}{2} \left( \frac{W}{L} \right)^2 (V_{GS2} - V_{th})^2 = \frac{\mu_p C_{ox}}{2} \left( \frac{W}{L} \right)^4 (V_{SG4} - V_t)^2
\]

Since we already know that

\[
V_{GS1} = V_{GS2} \\
V_{SG3} = V_{SG4}
\]

we note that (3) and (5) do not contain any variables we haven’t already solved for. These equations are not sufficient to solve for \(V_{DS2}\) or \(V_{SD4}\). At this point, we realize that the channel length modulation effect must be taken into account in order to solve for \(V_{DS2}\) or \(V_{SD4}\). The channel-length modulation effect shows how the drain current in active/saturation depends on the drain-to-source voltage.

The following device cross-section diagram helps to explain the channel length modulation effect.

![Cross-section diagram of an NMOS transistor in active/saturation region.](image)

Figure 2: Cross-section diagram of an NMOS transistor in active/saturation region.

The depletion region is labeled by DR and the effective channel is shown in red. As the drain to source voltage goes up the depletion region increases. This effectively shortens the channel length. As a result, the effective channel length \(L_{eff}\) of the device is dependent on the voltage between the drain and source terminals. To account for this effect, the geometrical channel length \(L\) should be replaced by the effective channel length \(L_{eff}\). Alternatively, a simpler model includes the channel length modulation effect through a multiplicative correction factor.
where $\lambda$ (lambda) is a device parameter. Ideally, $\lambda$ is small, so that the correction factor is close to 1. Lambda is related to the Early voltage parameter ($V_A$) of a device by the following equation

$$V_A = \frac{1}{\lambda} \quad (8)$$

Returning to the problem of finding $V_{DS2}$ or $V_{SD4}$ in the two-stage op-amp of Fig.1, we re-write equations (3) and (5) to include the correction factor (7) as follows:

$$\frac{\mu_n C_{ox}}{2} \left( \frac{W}{L} \right)_1 (V_{GS1} - V_m)^2 (1 + \lambda_n V_{DS1}) = \frac{\mu_p C_{ox}}{2} \left( \frac{W}{L} \right)_3 (V_{SG3} - V_{th})^2 (1 + \lambda_p V_{SD3}) \quad (9)$$

$$\frac{\mu_n C_{ox}}{2} \left( \frac{W}{L} \right)_2 (V_{GS2} - V_m)^2 (1 + \lambda_n V_{DS2}) = \frac{\mu_p C_{ox}}{2} \left( \frac{W}{L} \right)_4 (V_{SG4} - V_{th})^2 (1 + \lambda_p V_{SD4}) \quad (10)$$

Taking into account (6), and dividing equations (9) and (10) yields the equality

$$\frac{1 + \lambda_n V_{DS1}}{1 + \lambda_n V_{DS2}} = \frac{1 + \lambda_p V_{SD3}}{1 + \lambda_p V_{SD4}} \quad (11)$$

This equality yields that our initial guess (2) was correct and that the following is true,

$$V_{DS1} = V_{DS2}$$
$$V_{SD3} = V_{SD4} = V_{SG3} \quad (12)$$

which means that the DC voltage at Node 1 is in our numerical example,

$$V_1 = V_{D2} = V_{DD} - V_{SG3} = 5 - 1.16 = 3.84 \text{V} \quad (13)$$

Moving on to the final stage of the operational amplifier, it has already been solved that:

$$I_{B2} = 100 \mu A$$
$$V_{SG6} = V_{SG3}$$
$$I_{D3} = I_{D4} = 5 \mu A \quad (14)$$

Setting $I_{D6} = I_{B2}$, and assuming that $V_{out} = 0$, it is easy to verify that both M6 and M7 are in active/saturation, which allows us to solve for the aspect ratio of M6,

$$\left( \frac{W}{L} \right)_6 = \frac{I_{D6}}{I_{D3}} \left( \frac{W}{L} \right)_3 = 400 \quad (15)$$
Finally, we note that M6 and M7 are in active/saturation if $V_{out} = 0$, but what guarantees this? How do we find $V_{out}$? To resolve this, we will again have to include the channel length modulation effect in the output circuit:

$$I_{D6} = I_{D7} \quad \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS7} - V_{th})^2 (1 + \lambda_n V_{DS7}) = \frac{\mu_p C_{ox}}{2} \left( \frac{W}{L} \right) (V_{SG6} - |V_{th}|)^2 (1 + \lambda_p V_{SD6}) \quad (16)$$

resulting in,

$$\lambda_n V_{DS7} = \lambda_p V_{SD6}$$

$$\lambda_n (V_{out} + V_{SS}) = \lambda_p (V_{DD} - V_{out}) \quad (17)$$

A graphical view of this solution is helpful in understanding why the channel length modulation effect is necessary to find the exact $V_{out}$ voltage. The following drawing shows the graphical solution for $V_{out}$ from $I_{D6} = I_{D7}$ without taking into account the channel width modulation effect.

![Graphical solution of $I_{D6} = I_{D7}$ without taking the channel-length modulation effect into account.](image)

Figure 3: Graphical solution of $I_{D6} = I_{D7}$ without taking the channel-length modulation effect into account.

$I_{D7}$ is shown in red and $I_{D6}$ is shown in blue, whereas the overlap, corresponding to the solution for $V_{out}$ is shown in purple. This shows that $V_{out}$ is not a distinct value but any one of a range of values.

Including the channel length modulation effect produces the graphical solution shown in Fig. 4.
This drawing shows how if the channel length modulation effect is accounted for a specific $V_{out}$ can be found. The specific solution for $V_{out}$ is a function of $\lambda_n$, $\lambda_p$, and the supply rails. Since the tolerances for the parameters $\lambda_n$, $\lambda_p$ are relatively large, and since it is not possible to “match” the lambda parameters of the NMOS device M7 and the PMOS device M7 precisely, it is not possible to design the opamp for a precise value of $V_{out} = 0$, when the two inputs are set to 0. This is one of the reasons the input offset voltage $V_{OS}$ for the op-amp is not equal to zero.