CMRR of a diff amp with current-mirror load

Differential-mode gain

\[ M_1 \quad M_2 \]

\[ M_3 \quad M_4 \]

\[ +V_{DD} \]

\[ M_8 \]

\[ M_5 \]

\[ I_{B1} = 10 \text{ \mu A} \]

\[ -V_{SS} \]

\[ +v_{id}/2 \]

\[ -v_{id}/2 \]
CMRR of a diff amp with current-mirror load

Common-mode gain

\[ I_{B1} = 10 \mu A \]
CMRR of a diff amp with current-mirror load

Common-mode gain

CMRR
Two-stage op-amp output resistance

\[ +V_{DD} = 5 \text{ V} \]

\[ R_B = 8.8 \text{ M}\Omega \]

\[ I_B = 1 \mu\text{A} \]

\[ M_1 \]

\[ M_2 \]

\[ ID_1 = 5 \mu\text{A} \]

\[ ID_2 = 5 \mu\text{A} \]

\[ (W/L)_{1,2} = 100 \]

\[ (W/L)_{3,4} = 20 \]

\[ (W/L)_5 = 10 \]

\[ (W/L)_6 = 400 \]

\[ (W/L)_7 = 100 \]

\[ M_3 \]

\[ M_4 \]

\[ M_5 \]

\[ M_6 \]

\[ M_7 \]

\[ M_8 \]

\[ (W/L)_8 = 1 \]

\[ I_{B1} = 10 \mu\text{A} \]

\[ I_{B2} = 100 \mu\text{A} \]

\[ -V_{SS} = -5 \text{ V} \]

\[ IB = 1 \mu\text{A} \]

\[ IB_1 = 10 \mu\text{A} \]

\[ IB_2 = 100 \mu\text{A} \]

\[ ID_1 = 5 \mu\text{A} \]

\[ ID_2 = 5 \mu\text{A} \]
Basic (class-A) output stage
Common-drain (source follower) amplifier

\[ +V_{DD} = 5 \text{ V} \]

\[ R_B = 8.8 \text{ M} \Omega \]

\[ I_B = 1 \mu\text{A} \]

\[ I_{D1} = 5 \mu\text{A} \]

\[ I_{D2} = 5 \mu\text{A} \]

\[ (W/L)_{1,2} = 100 \]

\[ (W/L)_{3,4} = 20 \]

\[ (W/L)_{5} = 10 \]

\[ (W/L)_{6} = 400 \]

\[ (W/L)_{7} = 100 \]

\[ -V_{SS} = -5 \text{ V} \]
Basic (class-A) output stage
Common-drain (source follower) amplifier

$R_B = 8.8 \, \text{M}\Omega$

$I_B = 1 \, \mu\text{A}$

$I_{D1} = 5 \, \mu\text{A}$

$I_{D2} = 5 \, \mu\text{A}$

$M_1$

$(W/L)_{1,2} = 100$

$(W/L)_{3,4} = 20$

$M_3$

$M_4$

$V_{DD} = 5 \, \text{V}$

$V_{SS} = -5 \, \text{V}$

$M_5$

$(W/L)_{5} = 10$

$M_6$

$(W/L)_{6} = 400$

$M_7$

$(W/L)_{7} = 100$

$M_8$

$(W/L)_8 = 1$
Source follower gain and output resistance
Output voltage swing

\[ R_B = 8.8 \, \text{M}\Omega \]

\[ I_B = 1 \, \mu\text{A} \]

\[ I_{D1} = 5 \, \mu\text{A} \]

\[ I_{D2} = 5 \, \mu\text{A} \]

\[ (W/L)_{3,4} = 20 \]

\[ (W/L)_{1,2} = 100 \]

\[ (W/L)_5 = 10 \]

\[ (W/L)_7 = 100 \]

\[ +V_{DD} = 5 \, \text{V} \]

\[ -V_{SS} = -5 \, \text{V} \]

\[ M_1 \]

\[ M_2 \]

\[ M_3 \]

\[ M_4 \]

\[ M_5 \]

\[ M_6 \]

\[ M_7 \]

\[ M_8 \]

\[ M_9 \]

\[ M_{10} \]

\[ M_{11} \]

\[ M_{12} \]
Body effect

NMOS and PMOS transistor in a “vanilla” N-well CMOS process
Body effect: large-signal model
Body effect: small-signal model
Op-amp in N-Well CMOS process

\[ R_B = 8.8 \, \text{M}\Omega \]

\[ I_B = 1 \, \mu\text{A} \]

\[ I_{D1} = 5 \, \mu\text{A} \]

\[ (W/L)_{1,2} = 100 \]

\[ (W/L)_{3,4} = 20 \]

\[ (W/L)_5 = 10 \]

\[ (W/L)_6 = 400 \]

\[ (W/L)_7 = 100 \]

\[ +V_{DD} = 5 \, \text{V} \]

\[ -V_{SS} = -5 \, \text{V} \]

\[ M_1 \]

\[ M_2 \]

\[ M_3 \]

\[ M_4 \]

\[ M_5 \]

\[ M_6 \]

\[ M_7 \]

\[ M_8 \]

\[ M_9 \]

\[ M_{10} \]

\[ M_{11} \]

\[ M_{12} \]
Source follower gain and output resistance including body effect
PMOS source follower (in N-well CMOS process)

- $R_B = 8.8 \, \text{M} \Omega$
- $I_B = 1 \, \mu\text{A}$
- $I_{D1} = 5 \, \mu\text{A}$
- $I_{D2} = 5 \, \mu\text{A}$
- $I_{B1} = 10 \, \mu\text{A}$
- $I_{B2} = 100 \, \mu\text{A}$
- $V_{DD} = 5 \, \text{V}$
- $V_{SS} = -5 \, \text{V}$

$W/L_{1,2} = 100$
$W/L_{3,4} = 20$
$W/L_{5} = 10$
$W/L_{6} = 400$
$W/L_{7} = 100$
PMOS source follower (in N-well CMOS process)

\[ +V_{DD} = 5 \text{ V} \]

\[ R_B = 8.8 \text{ M} \Omega \]

\[ I_B = 1 \mu\text{A} \]

\[ I_{D1} = 5 \mu\text{A} \]

\( (W/L)_{1,2} = 100 \)

\[ (W/L)_{3,4} = 20 \]

\[ (W/L)_5 = 10 \]

\[ (W/L)_6 = 400 \]

\[ (W/L)_{7} = 100 \]

\[ I_{B1} = 10 \mu\text{A} \]

\[ I_{B2} = 100 \mu\text{A} \]

\[ I_{D2} = 5 \mu\text{A} \]

\[ (W/L)_8 = 1 \]
ECEN4827/5827

Introduction to 0.35u CMOS process
Spice models and Spice simulations using LTspice
Typical CMOS process (minimum channel length: 0.35μm)

- \( p \) substrate
- \( p \) well (body) for NMOS transistors, \( n \) well (body) for PMOS transistors
- \( n^+ \) and \( p^+ \) source/drain diffusions
- 1 or more polysilicon layers (2 POLY layers in this example)
- 2 or more metal layers (4 metal layers in this example)
Spice model library: 5827_035.lib

**NMOS**

NMOS transistor
B (p substrate) must be tied to most negative supply rail

**PMOS**

PMOS transistor
B is n-well, usually most positive supply rail

**RPN**

R_{sheet} = 1.2 k\Omega/square, TC = -400 ppm/°C
“square” = L/W

**RPP**

R_{sheet} = 50 \Omega/square, TC = +830 ppm/°C
“square” = L/W

**WDIODE**

Unit-area (5\mu\text{*}5\mu) p+ diffusion to n-well diode
n = area multiple. Cathode must be tied to the most negative supply rail
Example: NMOS model

```
*subckt MM D G S B
+params: W=10u L=1u
M1 D G S B MM L={L} W={W} AS={2u+W} PS={2*(2u+W)} AD={2u+W} PD={2*(2u+W)}
.ends

* NMOS transistor model
* MODEL NM NMOS LEVEL-0
* **************************************** SIMULATION PARAMETERS ****************************************
* format: LITspice
* model: MOS BSIMv3
* TYPICAL MEAN CONDITION
* *** Flags ***
+NOHMOD =1.000e+00 CAPMOD =2.000e+00
+NOFIMOD =3.000e+00
* *** Threshold voltage related model parameters ***
+K1 =5.0296e-01
+K2 =3.3985e-02 K3 =-1.136e+00 K3B =-4.399e-01
+CH =2.611e+17 UTH0 =4.979e-01
+VFF =-0.925e-02 DUT0 =5.000e+01 DUT1 =-1.839e+00
+DUT2 =-8.375e-03 KETA =2.632e-02
+PSREF1 =3.518e+00 PSREF2 =7.807e-05
```

… more (BSIM3 model is very detailed and complicated)…

- W, L are circuit design parameters, minimum 0.35μ, minimum increment 0.1μ
- NMOS Spice model can be used as is a subcircuit, which allows automatic adjustments of AS (source area), PS (source perimeter), DS (drain area) and PD (drain perimeter) as functions of W, or as a native MOS device (user must then manually specify AS, PS, DS, PD)
- Very detailed BSIM3 model (industry standard)
Approximate models for hand calculations

\( V_{tn} \approx 0.48 \text{ V} \)
\( \mu_n C_{ox} \approx 90 \mu \text{A/V}^2 \)
\( \lambda_n \approx 0.035 \text{ 1/V } (L=1\mu) \)
\( 0.025 \text{ 1/V } (L=2\mu) \)
\( <0.015 \text{ 1/V } (L>4\mu) \)

\( V_{tp} \approx -0.62 \text{ V} \)
\( \mu_p C_{ox} \approx 36 \mu \text{A/V}^2 \)
\( \lambda_p \approx 0.046 \text{ 1/V } (L=1\mu) \)
\( 0.019 \text{ 1/V } (L=2\mu) \)
\( <0.01 \text{ 1/V } (L>4\mu) \)

Beware: do not expect very accurate results using hand calculations, especially for short channel lengths \((L < 2 \mu)\)
Setting up 0.35u CMOS symbols and model library for LTspice

Option 1: local (does not require administrative privileges)

- Place all symbol files (*.asy files) and model library (5827_035.lib) in a working folder, together with schematics

Option 2: make symbols and model library globally available

- Place all symbols (*.asy files) in a new folder (e.g. 5827) in
  C:\Program Files\LTC\SwCAD\lib\sym
- Add model library 5827_035.lib to
  C:\Program Files\LTC\SwCAD\lib\sub

In any case, an LTspice schematic must include:

.lib 5827_035.lib
LTspice schematic entry

Run simulation

Enter component

Enter Spice “dot” commands

include 5807_035.lib library

.lib 5827_035.lib

VDD
3.3V

1.5V AC 1

M1
W=3u L=0.35u

M2
W=6u L=0.35u

.tran 0 100n 0.1n
.ac dec 101 1k 1g
dc Vin 0 3.3 0.01

in

out
Use of NMOS symbol in LTspice

(1) place `nmos_035` symbol

(2) **CTRL-right click** to open Attribute Editor

(3) Change **Prefix to X** to use subcircuit model with automatic adjustments of AS, PS, AD, PD

The same applies to `pmos_035`
Basic Spice simulations

Bias Point (.op)

- View DC operating point voltages and currents, and device small-signal model parameters in (text)

DC Sweep (.dc)

- Plot DC (or temperature) characteristics

AC Sweep (.ac)

- Plot small-signal frequency responses

Transient (.tran)

- Plot large-signal (total) waveforms
DC sweep example: inverter $V_{OUT}$ versus $V_{IN}$
AC sweep example: inverter as an amplifier, magnitude response $\|v_{out}/v_{in}\|$ [dB]
Transient example: inverter $v_{OUT}(t)$ for pulsating $v_{IN}(t)$
Hierarchical schematic entry

Inverter circuit with ports labeled (using Edit, Label Net, or F4 key)

Symbol representing the inverter circuit

Symbols used to enter larger circuits

inverter_035_1.asc

names must match

inverter_035_1.asy

test_inverter_035_1.asy