HW7 due by 10am MT On Friday Oct. 18
Includes design problems with extra-credit opportunities
Temperature dependences

Threshold voltage, \( TC_F(V_t) \approx -3000 \text{ ppm/oC} \)

Resistors

Positive and negative TC resistors are available

Example 0.35u CMOS process: -400ppm/oC and +830ppm/oC

Mobility, and MOSFET conductance parameter \( TC_F(\mu C_{ox}) \approx -5000 \text{ ppm/oC} \)

Forward biased pn-junction (\( V_{EB}, V_{BE} \) or \( V_D \)), -2mV/oC

Thermal voltage \( V_T = kT/q = 26\text{mV at 300}\text{oK}, +3300\text{ppm/oC at room temperature} \)
Introduction to bandgap references

Idea: a combination of forward-biased pm junction voltage and a voltage proportional to the thermal voltage $V_T = kT/q$ can result in ideally zero temperature coefficient at one temperature

$$V_{REF} = V_{EB \text{ \ junction\ \ voltage}} + \alpha \cdot V_T$$

$$\frac{\partial V_{REF}}{\partial T} = -2\frac{mV}{^\circ C} + \alpha \cdot (+87\frac{mV}{^\circ C})$$

$$V_T = \frac{kT}{q} \quad \frac{\partial V_T}{\partial T} = \frac{k}{q} = \frac{V_T}{T}$$

$$\frac{\partial V_{REF}}{\partial T} = 0$$

Choose $\alpha = \frac{2\frac{mV}{^\circ C}}{87\frac{mV}{^\circ C}} = 23$. 

ECEN4827/5827 Analog IC Design
pn-junction in an n-well process

\[ V_{EB} = V_T \ln \left( \frac{I}{I_S} \right) \]

- \( V_{EB} \) most negative supply rail.

\[ I = I_S \left( e^{V_{EB}/V_T} - 1 \right) \]

\[ V_{EB} = V_T \frac{kT}{q} \]

\[ I \approx I_S \]

\[ p \text{ substrate.} \]

area \( A = \pi \cdot (25 \mu m^2) \)

\[ WD\text{iode component in 0.35\mu CMOS process.} \]
How to obtain voltage proportional to $V_T$?

$$\Delta V_{EB} = V_{EB1} - V_{EB2}$$

$$\Delta V_{EB} = V_T \ln\frac{I_1}{I_{S1}} - V_T \ln\frac{I_2}{I_{S2}}$$

$$\Delta V_{EB} = V_T \ln\frac{I_1}{I_{S1}} \cdot \frac{I_{S2}}{I_2}$$

$$\Delta V_{EB} = V_T \ln\left(\frac{I_1}{I_2} \cdot n\right)$$

$I_1 = m \cdot I_2$ (e.g. mirror)

$\Delta V_{EB} = V_T \ln\left(\frac{I_1}{I_2} \cdot n\right)$

PTAT

(prop. to abs. temperature)

$\Delta V_{EB}$ independent of $I_{S1}$

(I1, I2 on same die)

matched

same temperature
A bandgap reference circuit example

Assume all $AS$, $V_{DD}$ large enough.

\[ I = \frac{V_{DD}}{L} = \frac{W}{L} \]

\[ I_1 = I_2 = I \]

\[ V_{GS1} + V_{EB1} = V_{GD2} + R_b I + V_{EB2} \]

\[ V_{EB1} - V_{EB2} = R_b I \]

\[ V_T \ln(n) = R_b I \]

\[ I = \frac{V_T}{R_b} \ln(n) \]

\[ V_{REF} = V_{EB} + d \cdot V_T \]

\[ R_b I + V_{EB2} = V_{EB2} + \frac{V_T \ln(n)}{d} \]

\[ d = 2^3, \quad n = e^d = e^8 \]
A bandgap reference circuit example

\[ I = \frac{V_T}{R_b} \ln n \]

\[ V_{\text{REF}} = V_{EB} + \frac{V_T}{R_b} (\ln n) \cdot kR_b \]

\[ V_{\text{REF}} = V_{EB} + \left( \frac{k \ln n}{\alpha} \right) \cdot V_T \]

\[ n > 1 \quad n = 8, 2^y, \ldots \]