ECEN4827/5827 lecture 25

- Review Design Problem D.1
- Continue analysis of frequency responses

Design problem D.1 was assigned to ECEN5827 students. All students are advised to review the problem and the solution posted on D2L. This circuit will be used as a building block in designs coming up later in the semester.
Design problem D.1

Wide-swing cascode PMOS current mirrors

Wide-swing cascode NMOS current mirrors

\[ \text{vp} = V_{DD} \]

\[ \text{vp} = 0 \text{, M}_2 \text{ "on"} \]

\[ \text{M}_2 \text{ is in deep triode} \]

\[ \text{V}_{SD} \approx 0 \]
Initial considerations and hand calculations

- To reduce channel-length modulation effects and increase output resistance, choose \( L = 3u \) for all transistors. A longer \( L \) also reduces current-mirror mismatches.

- A wide-swing cascode allows a minimum voltage of \( 2(V_{GS} - V_t) \). This voltage should be less than 0.5 V (specification (4)). Conservatively, choose (W/L)’s so that all transistors operate at \( V_{GS} - V_{tn} = V_{SG} - |V_{tp}| = 0.2 \) V. A larger \( V_{GS} - V_{tn} \) also reduces current-mirror mismatches.

- For the Vt-based current reference choose RPN resistor as \( R_b \) since it has higher resistance per square (1.2 k\( \Omega \)/square)

- Set the reference current to 1 \( \mu A \) so that the mirrors to output currents 1 \( \mu A \) and 10 \( \mu A \) can be done easily: \( I = V_{SG}/R_b = (0.2V+0.62V)/R_b = 1 \mu A \), \( R_b = 0.82 \) M\( \Omega \). Need \( 820/1.2 = 683 \) squares, so choose width \( WR = 1u \), length \( LR = 683u \)

- For all NMOS transistors, except the wide-swing cascode bias NMOS, we have:

\[
V_{GS} - V_{tn} = \sqrt{\frac{I}{K}} = 0.2 \text{ V, } K = \frac{\mu_n C_{ox} W}{2L} = \frac{I}{0.04} = 25 \mu A / V^2, \frac{W}{L} = 0.55, \text{ select } W = 2 \mu, \frac{W}{L} = 0.67
\]

- Similarly, for PMOS transistors, \( \frac{W}{L} = 50/36=1.4 \), select \( W = 4 \mu \).

- The wide-swing cascode bias transistors should have \( (W/L)_{bias} = (1/4)(W/L) \). Hence choose \( L = 4*3u = 12u \) for the bias transistors.
Use .param Spice directive to make it easy to adjust circuit parameters: LR (length of Rb resistor), L (length of all transistors), WN (width of NMOS transistors), and WP (width of all PMOS transistors).

Only the current reference portion of the circuit is shown here.

Bias NMOS for the wide-swing cascode.

Start-up circuit, just to make sure DC bias solution is ok.

Bias NMOS for the wide-swing cascode.

File: D1s.asc

Use F4 key to label node voltages for easy reference.

Value of parameter WP is specified as {WP}.
Bias voltage V(a) is 0.81 V, which means that the minimum output voltage for the cascode is 0.81-Vtn = approx. 0.33 V, which is less than 0.5 V (ok)

VDS of M8 and M10 is 0.12 V, which is lower than designed value (0.2 V); M8 and M10 may be in triode. This is because W/L is larger than ideal, and because the threshold of M7 and M9 is increased due to the body effect.

Start-up diode current is negligibly small (ok)

Output current is 11.3 uA, close to the hand calculated value, but 13% (> 5%) higher than the target (10 uA). So, increase LR to get the output current closer to 1uA; use parametric sweep to determine LR – see next page.
Use parametric sweep to select LR

$L = \frac{1}{2} LR^2$

Runs simulations over a range of LR from 700u to 800u in 1u steps
Parametric sweep: $I_{out}$ as a function of LR (for $V_p = 3.3$ V)

The output current is within 5% of 10μA for $731\mu < LR < 798\mu$. Next, check $I_{out}$ for $V_p = 0$ V
Parametric sweep: $I_{out}$ as a function of $LR$ (for $V_p = 0$ V)

The output current is within 5% of 1μA for $705\mu < LR < 771\mu$.
Select $LR = 750\mu$ (meets 5% spec for both cases)
Candidate design

LR=750u

Parametric sweep commented out

Next: repeat .op simulation to check the DC bias operating point
### .op (operating point) simulation (Vp = 3.3 V)

<table>
<thead>
<tr>
<th>Variable</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(d)</td>
<td>0.11844</td>
<td>voltage</td>
</tr>
<tr>
<td>V(b)</td>
<td>0.653882</td>
<td>voltage</td>
</tr>
<tr>
<td>V(a)</td>
<td>0.795711</td>
<td>voltage</td>
</tr>
<tr>
<td>V(f)</td>
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<td>voltage</td>
</tr>
<tr>
<td>V(vdd)</td>
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<td>voltage</td>
</tr>
<tr>
<td>V(e)</td>
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<td>voltage</td>
</tr>
<tr>
<td>V(c)</td>
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<td>voltage</td>
</tr>
<tr>
<td>V(n002)</td>
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<td>voltage</td>
</tr>
<tr>
<td>V(n003)</td>
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<td>voltage</td>
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<tr>
<td>V(ap)</td>
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<td>voltage</td>
</tr>
<tr>
<td>V(n004)</td>
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<tr>
<td>V(bp)</td>
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<tr>
<td>V(dn)</td>
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<td>V(on)</td>
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<tr>
<td>V(cp)</td>
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<td>V(dp)</td>
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<td>voltage</td>
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<td>V(op)</td>
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<td>V(p)</td>
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<tr>
<td>I(Vpdc)</td>
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<td>I(Vo)</td>
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<td>Ix(m10:D)</td>
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<td>Ix(m10:G)</td>
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</tr>
<tr>
<td>Ix(m8:B)</td>
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</tr>
</tbody>
</table>

Bias voltage V(a) is still very close to 0.8 V (ok)

VDS of M8 and M10 is 0.12 V, need to check triode/saturation

The output current for Vp=3.3V is Iout = -10.2 uA
The output current for Vp=0V is Iout = 0.98 uA (see next page)

The design meets spec 3.
.op (operating point) simulation (Vp = 0 V)

V(d): 0.11844 voltage
V(b): 0.653882 voltage
V(a): 0.795711 voltage
V(f): 2.42421 voltage
V(vdd): 3.3 voltage
V(e): 1.3638 voltage
V(c): 0.117643 voltage
V(n002): 1.1 voltage
V(n003): 0.119278 voltage
V(ap): 2.25533 voltage
V(n004): 0.119418 voltage
V(bp): 2.40585 voltage
V(dn): 5.83481e-010 voltage
V(on): 8.66997e-010 voltage
V(cp): 3.16698 voltage
V(dp): 3.16614 voltage
V(op): 1.51024 voltage
V(out): 1.5 voltage
V(p): 0 voltage
V(n001): 0 voltage
I(D1): 1.2864e-009 device_current
I(Vpdc): -6.31089e-030 device_current
I(Vo): 9.80068e-007 device_current
I(Vp): -6.31089e-030 device_current
I(Vstart): -1.2864e-009 device_current
I(Vdd): -5.86269e-006 device_current
Ix(m10:D): 9.74981e-007 subckt_current
Ix(m10:G): -8.83524e-029 subckt_current
Ix(m10:S): -9.74981e-007 subckt_current
Ix(m10:B): -1.1848e-013 subckt_current
Ix(m5:D): -9.80377e-007 subckt_current
Ix(m5:G): 0 subckt_current
Ix(m5:S): 9.80374e-007 subckt_current
Ix(m5:B): 2.50501e-012 subckt_current
Ix(m3:D): -9.74983e-007 subckt_current
Ix(m3:G): 0 subckt_current
Ix(m3:S): 9.74981e-007 subckt_current
Ix(m3:B): 1.93692e-012 subckt_current
Ix(m4:D): -9.73102e-007 subckt_current
Ix(m4:G): 3.02923e-028 subckt_current
Ix(m4:S): 9.73099e-007 subckt_current
Ix(m4:B): 3.52335e-012 subckt_current
Ix(m8:D): 9.73102e-007 subckt_current
Ix(m8:G): -7.57306e-029 subckt_current
Ix(m8:S): -9.73101e-007 subckt_current
Ix(m8:B): -1.17683e-013 subckt_current

VDS of M8 and M10 is 0.12 V, need to check triode/saturation (next page)

The output current for Vp=3.3V is Iout = -10.2 uA
The output current for Vp=0V is Iout = 0.98 uA

The design meets spec 3.

The IDD current is 5.86 uA, so the power dissipation for this design is 19.3 uW.
Check device parameters (View – Spice Error Log)

<table>
<thead>
<tr>
<th>Name</th>
<th>m:m20:1</th>
<th>m:m6:1</th>
<th>m:m9:1</th>
<th>m:m7:1</th>
<th>m:m8:1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model</td>
<td>nm</td>
<td>nm</td>
<td>nm</td>
<td>nm</td>
<td>nm</td>
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<tr>
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<tr>
<td>Vgs</td>
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<td>7.96e-01</td>
<td>6.77e-01</td>
<td>6.78e-01</td>
<td>6.54e-01</td>
</tr>
<tr>
<td>Vds</td>
<td>1.19e-01</td>
<td>7.96e-01</td>
<td>1.25e+00</td>
<td>5.36e-01</td>
<td>1.18e-01</td>
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<tr>
<td>Vbs</td>
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<td>0.00e+00</td>
<td>-1.18e-01</td>
<td>-1.18e-01</td>
<td>0.00e+00</td>
</tr>
<tr>
<td>Vth</td>
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<td>5.43e-01</td>
<td>5.43e-01</td>
<td>5.08e-01</td>
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<tr>
<td>Vdsat</td>
<td>1.21e-01</td>
<td>2.14e-01</td>
<td>1.17e-01</td>
<td>1.18e-01</td>
<td>1.21e-01</td>
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<tr>
<td>Gm</td>
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<td>6.14e-06</td>
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<td>1.17e-05</td>
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<td>Gds</td>
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<td>2.62e-08</td>
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<tr>
<td>Gmb</td>
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<td>1.73e-06</td>
<td>3.28e-06</td>
<td>3.26e-06</td>
<td>2.99e-06</td>
</tr>
</tbody>
</table>

VDS of M8 (and M10) is just slightly less than VDSat (which is the triode/saturation boundary voltage), so M8 and M10 are in triode but very close to saturation. This should not adversely affect the output resistance, so we can keep the design as is.

Note that device small-signal parameters $G_m = gm$, $G_{ds} = 1/ro$, and $G_{mb} = gmb$ are computed at the DC-operating point.
Sensitivity analysis (approximate hand calculations)

Output currents are scaled copies of $I_{ref}$, hence it is sufficient to look at this part of the circuit and find the sensitivity

$$S_{VDD}^{I_{ref}} = \frac{V_{DD}}{I_{ref}} \frac{i_{ref}}{v_{dd}}$$

Need to find this gain by small-signal analysis
Sensitivity analysis (approximate hand calculations)

This was found in class for the Vt-based reference with cascode mirror:

\[ I_{\text{ref}} = \frac{1}{g_{m3} R_b (g_{m9} r_9 r_{10})} \cdot V_{dd} \]

Unfortunately, there is another signal path, which results in higher sensitivity, approximately:

\[ I_{\text{ref}} = \frac{1}{r_{o5} g_{m6} r_{10}} \cdot V_{dd} \]
Sensitivity analysis (approximate hand calculations)

\[ i_{ref} = \frac{1}{r_{o5} g_{m6} r_{o10}} v_{dd} \]

From .op simulation (see Spice Error Log):

\( r_{o5} = 1/8.47e-09 = 118 \text{ M}\Omega \)
\( r_{o10} = 1/2.34e-06 = 0.427 \text{ M}\Omega \)
\( g_{m6} = 6.14e-06 \)

\[ S_{VDD}^{I_{ref}} = \frac{V_{DD}}{I_{ref} v_{dd}} = 0.011 \]
Sensitivity analysis by simulations

There are several possible approaches to find $\Delta i_{\text{out}}/\Delta V_{\text{DD}}$ in order to compute sensitivity:

1. Run `.op` analysis for $V_{\text{DD}} = 3.3$ V, and for a slightly higher $V_{\text{DD}} + \Delta V_{\text{DD}}$ (for example, $\Delta V_{\text{DD}} = 0.1$ V). Find the corresponding change in $i_{\text{out}}$.

2. Run a `.dc` sweep of $V_{\text{DD}}$ from 3.3 V to $3.3 + \Delta V_{\text{DD}}$, plot $i_{\text{out}}$ and find $\Delta i_{\text{out}}$.

3. Run an `.ac` analysis to find the small-signal gain $i_{\text{out}}/v_{\text{dd}}$ at low frequencies. This approach was suggested in the problem, in order to emphasize the point that finding $i_{\text{out}}/v_{\text{dd}}$ is a small-signal problem. In this case, there is no need to guess how small $\Delta V_{\text{DD}}$ should be.

4. Run transfer function (`.tf`) analysis to find the small-signal gain $i_{\text{out}}/v_{\text{dd}}$ at zero frequency. This is the easiest approach: the results are shown on the next page.
### Sensitivity analysis by .tf simulations

![tf simulation](image)

<table>
<thead>
<tr>
<th>Vp = 0 V</th>
<th>Vp = 3.3 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>--- Transfer Function ---</td>
<td>--- Transfer Function ---</td>
</tr>
<tr>
<td>Transfer_function: 4.72472e-009</td>
<td>Transfer_function: -3.2606e-008</td>
</tr>
</tbody>
</table>

\[ S_{VDD}^{I_{out}} = \frac{V_{DD}}{I_{out}} \frac{i_{out}}{v_{dd}} = 0.016 \]

\[ S_{VDD}^{I_{out}} = \frac{V_{DD}}{I_{out}} \frac{i_{out}}{v_{dd}} = 0.011 \]
DC sweep ($V_p = 3.3V$)

Total change is $44nA/10uA = 0.44\%$, well within allowed $\pm 0.5\%$
DC sweep \((Vp = 0V)\)

Total change is \(4.2\text{nA}/1\mu\text{A} = 0.42\%\), well within allowed +/-0.5%

The design meets spec 4
Temperature sweep (Vp = 3.3 V)

.output temp 0 70 1

Output current temperature coefficient is negative, as expected
Temperature sweep (Vp = 0 V)

Output current temperature coefficient is negative, as expected.
Transient simulation

The waveform is generally as expected, except for the large spikes at the transitions.
Spikes in the output current

When M1 is off (Vp = 0), this voltage drops to zero. When Vp=3.3 is applied, VGS(M1)=3.3V initially, resulting in a large current spike until the capacitance at this node is charged up so that the voltage increases and M14, M13 limit the current to 10uA. The same reasoning applies to M2, M19, M18.
An improvement (file: D1s_improved.asc)

M1, M22 and M2, M23 operate as differential pairs.

When M1 is off, M22 conducts the cascode current; the voltage swing here is smaller. Similarly, when M2 is off, M23 conducts the PMOS cascode current.
Transient simulation of the improved circuit

The spikes have been reduced by about 50% in amplitude. Also, the transients are shorter.
Back to analysis of frequency responses
MOS transistor model with capacitances

Complete small-signal model.
CS amplifier frequency responses

Assume DC bias such that $M_1, M_2$ are AS

Model of the previous stage

Small-signal input

DC bias

$V_{i+i}$

$R_{in}$

$V_{o+vo}$

$+V_{DD}$

$C_{gs2} + C_{gs3}$

$C_{gd2}$

$C_{gd1}$

$C_{gs1}$

$C_{ab2}$

$C_{ab1}$

$M_1$

$M_2$

$M_3$

$CL$

Input cap of the next stage

Model of the next stage

Out resistance of the prev. stage

ECEN4827/5827 Analog IC Design
CS amplifier SSM and frequency response

**Numerical Example:**
- \( g_{m1} = 500 \mu A/V \)
- \( R_{o1} = R_{o2} = 400 \, k\Omega \)
- \( R_{in} = 200 \, k\Omega \)
- \( C_{gs1} = 0.27 \, pF \)
- \( C_{gd1} = 0.02 \, pF \)
- \( C_{db1} = C_{db2} = 0.12 \, pF \)
- \( C_L = 0.2 \, pF \)

**Eqn:** \( A(s) = \frac{V_o}{V_i} \)

\[ R_{in} \]
\[ C_{gd1} \]
\[ C_{gs1} \]
\[ g_{m1} V_{gs1} \]
\[ R_2 \]
\[ V_i \]
\[ V_{gs1} \]
\[ C_L \]

\[ V_o \]

\[ R_2 = R_{o1} || R_{o2} \]
CS amplifier $A(s)$

\[
\frac{v_i - v_{gs1}}{R_{in}} = sC_{gs1} v_{gs1} + sC_{gd1} (v_{gs1} - v_o)
\]

\[
sC_{gd1} (v_{gs1} - v_o) = g_{m1} v_{gs1} + \frac{v_o}{R_2} + sC_2 v_o
\]

\[
A(s) = \frac{A(0)}{1 + a_1 s + a_2 s^2}
\]

Order = 2 because 3 caps form a loop.
CS amplifier $A(s)$

$solution:\quad A(s) = A(0) \frac{1 + b_1 s}{1 + a_1 s + a_2 s^2} = A(0) \frac{1 - \frac{s}{\omega_2}}{(1 + \frac{s}{\omega_{f_1}})(1 + \frac{s}{\omega_{f_2}})}$

\[ b_1 = -\frac{C_{gd1}}{g_{m1}} \]

\[ a_1 = R_{in} C_{gs1} + R_2 C_2 + (R_{in} + R_2 + g_{m1} R_{in} R_2) C_{gd1} \]

\[ a_2 = R_{in} R_2 (C_{gs1} C_2 + C_{gs1} C_{gd1} + C_{gd1} C_2) \]

\[ A(0) = -g_{m1} R_2 \]

\[ R_2 = \frac{R_1}{R_2} \]

Numerical results:

- $A(0) = -100$ (40dB)
- $f_{f_1} = 300$ kHz
- $f_{f_2} = 16$ kHz
- $f_T = \frac{g_{m1}}{2\pi C_{gd1}} = 46$ kHz
- $f_{T_2}$
- RHP zero
- right-half-plane
CS amplifier magnitude response and BW

20 \log |A(j\omega)|[dB]

\[ 20 \log |A(j\omega)| = 20 \log |A(j\omega)|_{3dB} + 20 \log |A(j\omega)|_{3dB} \]

Bandwidth : \( (3dB) \)

\[ 20 \log |A(j\omega)|_{3dB} = 20 \log |A(j\omega)|_{3dB} - 3dB. \]

\[ B(s) = \frac{B(\omega)}{1 + \frac{s}{\omega_p}} \]

\[ BW = f_p = \frac{\omega_p}{2\pi} \]

\[ f_p \gg f_1 \]

\[ BW \approx f_1 \]

\[ f_2 \ll f_1 \]

\[ f_2 \ll f_1 \]

\[ f_2 \ll f_1 \]
Dominant pole approximation

\[ A(s) = A(0) \frac{1 + b_1 s}{1 + a_1 s + a_2 s^2} = A(0) \frac{1 - \frac{s}{\omega_2}}{(1 + \frac{s}{\omega_1})(1 + \frac{s}{\omega_2})} \]

Dominant pole: \( f_{p1} \ll f_{p2}, f_2 \) (\( f_{p1} \ll \) other poles and zeros frequencies).

\[ \text{BW [Hz]} \approx \frac{f_{p1}}{\omega_2} \]

\[ A(s) = A(0) \frac{1 - \frac{s}{\omega_2}}{1 + \left(\frac{1}{\omega_1} + \frac{1}{\omega_2}\right)s + \frac{1}{\omega_1 \omega_2} s^2} \]

\[ a_1 = \frac{1}{\omega_1} + \frac{1}{\omega_2} \approx \frac{1}{\omega_1} \quad (\omega_1 \ll \omega_2) \]

\[ \text{BW} \approx f_{p1} \approx \frac{1}{2\pi a_1} \quad \text{[Hz]} \]

\[ a_1 \text{ can be found without computing complete } A(s) \]