Dominant-pole compensation of the 2-stage CMOS op-amp

\[ (W/L)_{1,2} = 100 \]
\[ (W/L)_{3,4} = 20 \]
\[ (W/L)_{5} = 10 \]
\[ (W/L)_{7} = 100 \]

\[ I_B = 1 \mu A \]
\[ I_{B1} = 10 \mu A \]
\[ I_{B2} = 100 \mu A \]

\[ I_{D1} = 5 \mu A \]
\[ I_{D2} = 5 \mu A \]
2-stage CMOS op-amp model: $A(s)$ including $C_c$ and high-frequency dynamics
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Unity-gain feedback circuit: $T(s) = A(s)$
Phase margin, $f_c$, high-frequency pole, and RHP zero
RHP Zero Cancellation

\[ +V_{DD} = 5 \text{ V} \]

\[ I_B = 1 \mu A \]

\[ I_{D1} = 5 \mu A \]

\[ I_{D2} = 5 \mu A \]

\[ I_{B1} = 10 \mu A \]

\[ I_{B2} = 100 \mu A \]

\[ (W/L)_{3,4} = 20 \]

\[ (W/L)_{1,2} = 100 \]

\[ (W/L)_5 = 10 \]

\[ (W/L)_7 = 100 \]

\[ (W/L)_8 = 1 \]
RHP Zero Cancellation
RHP Zero Cancellation
RHP Zero Cancellation: Implementation

\[ I_{D1} = 5 \, \mu A \]

\[ I_{D2} = 5 \, \mu A \]

\( M_1 \)

\( M_2 \)

\( M_3 \)

\( (W/L)_{3,4} = 20 \)

\( (W/L)_{1,2} = 100 \)

\( I_{B1} = 10 \, \mu A \)

\( I_{B2} = 100 \, \mu A \)

\( I_B = 1 \, \mu A \)

\( +V_{DD} = 5 \, V \)

\( -V_{SS} = -5 \, V \)

\( (W/L)_8 = 1 \)

\( (W/L)_{5} = 10 \)

\( (W/L)_{7} = 100 \)

\( (W/L)_5 = 10 \)