Dominant-pole compensation of the 2-stage CMOS op-amp

2, 2 high resistance nodes w/ device capacitance having the largest effects

\[ V_{DD} = 5 \text{ V} \]

\[ I_{D1} = 5 \mu\text{A} \]

\[ I_{D2} = 5 \mu\text{A} \]

\[ I_{B1} = 10 \mu\text{A} \]

\[ I_{B2} = 100 \mu\text{A} \]

\[ V_{SS} = -5 \text{ V} \]

\[ (W/L)_{3,4} = 20 \]

\[ (W/L)_{1,2} = 100 \]

\[ (W/L)_{3} = 10 \]

\[ (W/L)_{7} = 100 \]

\[ C_1 = C_{jg1} + C_{d1b4} + C_{d1bL} \]

\[ C_2 = C_{d1bL} + C_{d1b7} + C_{load} \]

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We are now going to include parasitics from the devices which have the largest contribution.
2-stage CMOS op-amp model: $A(s)$ including $C_c$ and high-frequency dynamics

\[ V_{\text{in}} = V_{\text{gsf}} \]

\[ R_1 = R_\text{in} \parallel r_\text{in} \]

Same as CS amplifier

\[ A(s) = A(0) \frac{1+b_1 s}{1+a_1 s + a_2 s^2} = A(0) \frac{1 - \frac{s}{w_p}}{(1 + \frac{s}{w_{p1}})(1 + \frac{s}{w_{p2}})} \]

\[ A(0) = g_m R_1 R_2 \]

\[ b_1 = -\frac{(C_c + C_g s)}{g_m} \]

\[ a_1 = R_1 C_1 + R_2 C_2 + (C_c + C_g s)(R_1 + R_2 + g_m R_1 R_2) \]

\[ a_2 = R_1 R_2 (C_1 C_2 + C_1 (C_c + C_g s) + C_2 (C_c + C_g s)) \]

RHP zero will introduce a phase-lag, this is undesirable.
2-stage CMOS op-amp model: \( A(s) \) including \( C_c \) and high-frequency dynamics

\[
f_{p1} \approx \frac{1}{2\pi a_1} = \frac{1}{2\pi \left( C_c + C_{gds} \right) g_m R_1 R_2}
\]

\[
a_2 = \frac{1}{w_{p1} w_{p2}} \quad w_{p1} = \frac{1}{w_{p1} a_2} = \frac{a_1}{a_2}
\]

\[
f_{p2} \approx \frac{1}{2\pi a_2} = \frac{1}{2\pi \left( C_c + C_{gds} \right) g_m R_2} \left[ \frac{C_1 C_2 + C_i \left( C_c + C_{gds} \right) + C_o \left( C_c + C_{gds} \right)}{C_c + C_{gds}} \right]
\]

\[
f_{p3} = \frac{1}{2\pi} \frac{g_m}{C_1 + C_2 + \frac{C_i C_2}{C_c + C_{gds}}}
\]

\[
f_z = \frac{1}{2\pi} \frac{g_m}{C_c + C_{gds}}
\]

\( \text{RHP} \Rightarrow \text{ZC} \)

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\[ C_c \uparrow \]

\[ f_{p1} \downarrow \] \# get more separation \Rightarrow \text{called 'pole splitting'} \text{ good}

\[ f_{p2} \uparrow \]

\[ f_z \downarrow \] \text{Not good bc reduce phase margin}
2-stage CMOS op-amp model: $A(s)$ including $C_c$ and high-frequency dynamics

Unity gain gives worst case

$T(s) = A(s)$
Unity-gain feedback circuit: $T(s) = A(s)$

$C_C = \frac{1}{\omega} \text{op-amp} \text{ is uncompenated} \left(\omega_u\right)$

$\phi_u = 90^\circ - \tan^{-1} \frac{f_c}{f_{2u}}$

Likely $\phi_u < 0$ unstable.

$f_c = \text{GBW} = A(0) f_{p1}$

Consider $C_C$ & well

Chose $C_C$

After adding $C_C$
Phase margin, \( f_c \), high-frequency pole, and RHP zero

\[
P_m = 90^\circ - \tan^{-1} \left( \frac{f_c}{f_p} \right) - \tan^{-1} \left( \frac{f_c}{f_c} \right)
\]

\[
f_c = A(0) f_m = \frac{g_m}{2\pi (C_c + C_c)} \times \frac{g_m}{2\pi C_c}
\]

\[
P_m = 90^\circ - \tan^{-1} \left[ \frac{g_m}{2\pi C_c} \right] - \tan^{-1} \left[ \frac{g_m}{2\pi C_c} \right]
\]

\[
P_m = 90^\circ - \tan^{-1} \left( \frac{g_m}{g_m} \left( \frac{C_1 + C_2 + C_3}{C_c} \right) \right)
\]

- \( f_c \) has no contribution. Also, \( g_m \) small is necessary condition
- \( \frac{g_m}{g_m} \) large current
- Larger current in general here

Small \( g_m \), \( g_m > g_m \) is good

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RHP Zero Cancellation

$+V_{DD} = 5$ V

$I_{D1} = 5$ $\mu$A

$M_1$  

$\frac{(W/L)_{1,2}}{2} = 100$

$M_2$

$M_3$

$M_4$

$M_5$

$M_6$

$C_{ds}$

$C_{gc}$

$R_c$

$R_e = \frac{1}{g_{me}}$

$I_{B1} = 10$ $\mu$A

$I_{B2} = 100$ $\mu$A

$I_{D2} = 5$ $\mu$A

$I_{B} = 1$ $\mu$A

$(W/L)_{6} = 10$

$(W/L)_{7} = 100$

$-V_{SS} = -5$ V


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\[\text{RHP Zero Moves Down in freq as } C_C \text{ is added}\]
RHP Zero Cancellation

\[ \text{v_{in}} \rightarrow \text{gm}_{1}\text{v}_{\text{in}} \]

\[ R_{\text{nc}} = \frac{V_{\text{test}}}{I_{\text{test}}} \bigg|_{V_{o} \rightarrow 0} = - \frac{1}{\text{gm}_{o}} \]

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How can we eliminate this?

What should this resistance be?

Want \( R_{\text{nc}} = 0 \) \( \Rightarrow \) How can we make this happen?

We are starting with a \text{NEGATIVE} resistance

\[ R_{\text{nc}} = 0 = \frac{1}{\text{gm}_{1}} - \frac{1}{\text{gm}_{6}} \]

How is this resistance implemented?