Analog IC application areas

- Interface
  - A/D and D/A conversion
  - Filtering
  - Drivers & amplifiers
- Clock management, PLL’s
- Power management
  - Linear regulators
  - Switched-mode power conversion
- RF circuitry
Introduction to analog IC design in power management applications

- Power management application example: battery-powered mobile electronics
- Brief introduction to operation and steady-state analysis of PWM switched-mode power converters*
- Low-power monolithic DC-DC converter ICs: power MOSFETs and gate-drivers
- PWM controller architectures and analog IC building blocks
- Examples of PWM controller realizations: HW13 design problem

*ECEN5797 Introduction to Power Electronics provides in-depth coverage of this material
State-of-the-art portable applications, “smart phones”

- Much increased functionality
  - Voice, data communication
  - Applications
  - Audio, Video, Camera
  - Backlit touch-screen color display
- Multiple radios
  - High-speed wireless (3G=4G, e.g. WCDMA, LTE)
  - Wi-Fi, Bluetooth
  - GPS receiver
- Much increased processing power and data rates
- Much more activity in the usage model
- Severe impact on the battery life
Simplified system block diagram

Major power consumers: PA, baseband digital, display lighting, analog
Different voltage/current requirements

Basic power management:
- Efficient distribution of required voltage/current levels
- ON/OFF control for all functional blocks
Power distribution

Battery example: single-cell Lithium-Ion

Power distribution: $V_{bat} = 2.7-4.5$ V

Power supply choices: (1) nothing, (2) LDO, (3) switcher, or (4) switched-cap
Power for μP/DSP core

\[ P = CV_{DD}^2 f_c + V_{DD} I_{off} \]

- Dynamic or AC power: \( C(V_{DD})^2 f_c \)
- Static or DC or leakage power: \( V_{DD} I_{off} \)
- \( V_{DD} \) down to 1-2 V or less, load current up to several 100 mA

\( C \) constant proportional to the number of gates and switching activity
\( f_c \) clock frequency
\( I_{off} \) leakage current proportional to the number of gates, increases with reduced device threshold voltages \( V_{tn}, V_{tp} \)
Power Supply Example: Step-Down Voltage Regulator

Step-down regulators are used as power supplies for baseband digital core and the RF power amplifier (PA)
Efficiency

\[ \eta = \frac{\text{output DC power}}{\text{input DC power}} = \frac{P_o}{P_g} = \frac{V_o I_o}{V_g I_g} \]

\[ V_g = V_{bat} = \text{input DC (battery) voltage} \]
Linear voltage regulator as power supply

Series pass transistor

Simple, low noise, small footprint area
Output voltage lower than the battery voltage
High efficiency only if \( V_o \) is close to input voltage \( V_{bat} = V_g \)
Linear regulator power model

\[ I_g = I_o + I_Q \]

Efficiency:

\[ \eta = \frac{V_o I_o}{V_g I_g} = \frac{V_o I_o}{V_g (I_o + I_Q)} \]

Linear regulator efficiency cannot be greater than the ratio of the output and the input voltage

\[ \eta < \frac{V_o}{V_g} \]
Linear regulator efficiency example

Example:
\( V_g = 3.6 \text{ V} \)
\( V_o = 1.5 \text{ V} \)
\( I_Q = 50 \mu\text{A} \)
\( 0 < I_o < 300 \text{ mA} \)
Buck (step-down) switching power converter

Low-pass LC filter

\[ f_s = \frac{1}{T_s} \] = switching frequency

\[ D = \text{switch duty cycle} \]

**Conversion ratio:**

\[ M(D) = \frac{V_o}{V_g} = D \]
Steady-state waveforms

\[ \Delta i_L = \frac{V_g}{2L f_s} (1 - D)D \]

\[ \Delta v = \frac{V_g}{16 C L f_s^2} (1 - D)D \]
Switch-Mode Power Supplies

- Step-up, step-down and inverting configurations available
- Switching converters are ideally 100% efficient
- Real efficiency can be close to 100%; depends on operating conditions and implementation
- Converters generate switching noise
- Discrete filter components ($L, C$) are required
- Higher switching frequency $\Rightarrow$ smaller $L, C$
- Closed-loop output voltage control: switch duty cycle is the control variable
SMPS efficiency as a function of load

Example:
\[ V_{g} = 3.6 \text{ V} \]
\[ V_{o} = 1.5 \text{ V} \]
\[ 0 < I_{o} < 300 \text{ mA} \]
Impact of efficiency: a system example

<table>
<thead>
<tr>
<th>uP/DSP core mode</th>
<th>Stand-by</th>
<th>Wait</th>
<th>Run1</th>
<th>Run2</th>
<th>FullRun</th>
</tr>
</thead>
<tbody>
<tr>
<td>% of time in this mode</td>
<td>90.0</td>
<td>4.0</td>
<td>3.0</td>
<td>2.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Load current Io [mA]</td>
<td>0.1</td>
<td>1.0</td>
<td>10.0</td>
<td>100.0</td>
<td>300.0</td>
</tr>
</tbody>
</table>

| Linear regulator       | Efficiency [%] | 34.7  | 40.9  | 41.6  | 41.7  | 41.7  |
| Battery current Ig [mA]| 0.12      | 1.02  | 10.02 | 100.02| 300.02|
| Average Ig in this mode [mA]| 0.11   | 0.04  | 0.30  | 2.50  | 1.50   |

| Total linear reg average Ig [mA]| 4.45 |

| SMPS                          | Efficiency [%] | 29.1  | 78.4  | 93.7  | 93.0  | 87.7  |
| Battery current Ig [mA]       | 0.14      | 0.53  | 4.45  | 44.82 | 142.60|
| Average Ig in this mode [mA]  | 0.13      | 0.02  | 0.13  | 1.12  | 0.71   |

| Total SMPS average Ig [mA]    | 2.12 |

Example:

\[ V_g = 3.6 \text{ V} \]
\[ V_o = 1.5 \text{ V} \]
\[ 0 < I_o < 300 \text{ mA} \]
Impact of efficiency

- SMPS results in significantly lower average battery current
- High efficiency over a wide range of loads is important
- Low zero-load bias current $I_0$ is particularly important for mobile systems that spend significant amount of time in “stand-by” modes
Switch realization with a synchronous rectifier

“Synchronous Buck”

PMOS: main switch
NMOS: synchronous rectifier

Switch control signals

Dead times are used to prevent short-circuit current through PMOS/NMOS
“Non-synchronous Buck”

Switch realization with diode rectifier

PMOS: main switch

\[ V_g \]

\[ V_p \]

\[ v_p(t) \]

\[ i_p(t) \]

\[ i_L(t) \]

\[ v_L(t) \]

\[ i_C(t) \]

\[ I_o \]

\[ v(t) \]

The diode rectifier is an on-chip body diode or an external Schottky rectifier
Switch currents

Average and RMS values

\[ I_p = \langle i_p(t) \rangle \approx DI_o \]

\[ I_{p,rms} = \sqrt{\langle i_p^2(t) \rangle} \approx \sqrt{DI_o} \]

\[ I_n = \langle i_n(t) \rangle \approx (1-D)I_o \]

\[ I_{n,rms} = \sqrt{\langle i_n^2(t) \rangle} \approx \sqrt{1-DI_o} \]

Switch on-resistance and forward voltage drops result in switch conduction losses
Conduction-loss models

PMOS: On-resistance $R_{on,p}$

NMOS: On-resistance $R_{on,n}$

Diode: Forward voltage drop $V_D$ in series with on-resistance $R_D$

Inductor: Winding resistance $R_L$
Buck circuit when the PMOS is ON

\[ v_L = V_g - (R_{on,p} + R_L)i_L - v \approx V_g - (R_{on,p} + R_L)I_o - V \]

\[ i_g = i_L \approx I_o \]
Buck circuit when the rectifier is ON

\[ v_L = -(R_D + R_L)i_L - V_D - v \approx -(R_D + R_L)I_o - V_D - V \]

\[ i_g = 0 \]
Steady-state model with conduction losses

Inductor volt-second balance:

\[
\langle v_L \rangle = 0
\]

\[
V = DV_g - (DR_{on,p} + (1 - D)R_D + R_L)I_o - (1 - D)V_D
\]

Input current:

\[
I_g = \langle i_g \rangle = DI_o
\]

Equivalent steady-state circuit model with conduction losses:
Example: synchronous rectifier versus diode rectifier

- Given $V_g=3.6\text{V}$, $V_o=1.5\text{V}$, $I_o=300\text{mA}$
- Regulator A uses a PMOS switch with $R_{on,p}=0.4\Omega$ and a Schottky rectifier with $V_D=0.5\text{V}$, $R_D=0.1\Omega$.
- Regulator B uses a PMOS switch with $R_{on,p}=0.4\Omega$, and a synchronous rectifier with $R_{on,n}=0.5\Omega$.
- Ripples are small and other losses of the two regulators are comparable.
- Which regulator has higher efficiency?
Solution

Use the equivalent circuit model to find the duty cycle $D$:

\[ V = DV_g - (DR_{on,p} + (1-D)R_D + R_L)I_o - (1-D)V_D \]

Note: because of losses, the duty cycle is greater than ideal steady-state

\[ D = \frac{V}{V_g} \left( 1 + \frac{V_D + (R_D + R_L)I_o}{V} \right) \]

\[ \frac{V}{V_g} - \frac{(R_{on,p} - R_D)I_o - V_D}{V_g} \]
Find component losses, regulator A

\[ D = 0.54 \]

**PMOS:** \[ R_{on,p} DI_o^2 = 19mW \]

**Diode:** \[ R_D (1 - D) I_o^2 + (1 - D)V_D I_o = 73mW \]

**Inductor:** \[ R_L I_o^2 = 1mW \]

**Total conduction loss:** \[ P_{loss} = 93mW \]

**Efficiency (neglecting other losses):** \[ \eta = \frac{P_o}{P_o + P_{loss}} = 83\% \]
Find component losses, regulator B

\[ D = 0.46 \]

PMOS: \[ R_{on,p} DI_o^2 = 17\text{mW} \]

NMOS: \[ R_{on,n} (1 - D)I_o^2 = 19\text{mW} \]

Inductor: \[ R_L I_o^2 = 1\text{mW} \]

Total conduction loss: \[ P_{loss} = 37\text{mW} \]

Efficiency (neglecting other losses): \[ \eta = \frac{P_o}{P_o + P_{loss}} = 92\% \]

Conclusion: the synchronous buck regulator B has significantly lower conduction loss