Closed-loop (feedback) control

- The output voltage is compared to a bandgap reference $V_{ref}$
- The controller generates pulsating switch-control waveforms (p and n) to (ideally) null the error
- Bandgap design is critical for voltage-regulation and $I_Q$ specs
Voltage regulation objectives

Static voltage regulation

- DC output voltage precision, i.e., % variation (~ ±1% typical) with respect to the nominal value over:
  - input voltage range (“line regulation”)
  - output load range (“load regulation”)
  - process and temperature variations

Dynamic voltage regulation

- “Load transient response,” including peak output voltage variation and settling time for a step load transient
- “Line transient response,” including output voltage variation and settling time for a step input voltage transient
Two standard control approaches in constant-frequency PWM converters

Voltage-mode control

• The switch duty cycle is controlled based on output voltage sensing

Current-mode control

• The switch duty cycle is controlled based on output voltage \textit{and} switch current sensing
Voltage-Mode PWM Control Architecture

\[ v_g(t) \]

Power input

\[ v_L(t) \]

\[ v(t) \]

Load

\[ v_{sw}(t) \]

\[ v_c(t) \]

\[ G_c(s) \]

Compensator

\[ v_{ref} \]

Controller chip

\[ v(t) \]

Feedback connection

\[ i_L(t) \]

\[ L \]

\[ i_C(t) \]

\[ G_c(s) \]

Pulse-width modulator

\[ dT_s \]

\[ T_s \]

\[ t \]

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HW Buck Voltage Regulator

V_{in} = 1V

0.1 - 0.25A at 42pS.

0 - to - 0.15A

Step load at 42pS.

Gate drivers

dead-time circuit

d = switch dutycycle.

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