Design a fully differential version of the symmetrical CMOS OTA with CMFB based on the "two differential amp" approach to sensing the common-mode output and feeding back the bias current. The design should meet the following specifications:

- Low-frequency differential gain: $A_{vd} \geq 100$
- Differential gain-bandwidth: $GBW \geq 1MHz$
- Input common-mode range, ICMR: $1.5V \leq V_{IC} \leq 4.5V$
- Differential output slew-rate limit: $SR \geq 5V/\mu s$
- Output common mode regulated to: $V_{oc\_ref} = 2.5V$
- CMFB loop-gain cross-over frequency: $f_{c\_CMFB} \geq 1MHz$

With the following design constraints:

- Power supplies: $Vdd = 5V$, $Vss = 0V$
- Use only one ideal current source in your final design
- Use the model files from the AMIC5 process located in (as used in 4228/5008):
    - magellan:/usr/local/cadence/cadence/models/amic5/mos.scs Section: typ
- Area & power optimization are not critical: just get a design to meet the specs
- Note: use large device lengths in current mirrors to reduce channel-length modulation effects (without going to cascode designs), i.e. L=4u.
- Load capacitance: two single ended caps, $C_L = 5pF$, attached from each output to ground

<u>Turn in the following in a PowerPoint presentation file</u> via e-mail to the instructor by the due date. Use screen-capture images from cadence for schematics and simulation results. Do not print or turn in hardcopies.

- Full schematic of your design
- Simulation results verifying that each of the above design specifications have been met
- Simulation result showing the maximum differential output of the OTA before one of the devices in the CMFB circuit leaves the active operating mode
- Show how to increase the maximum differential output of the OTA allowed by the CMFB circuit. How does your improvement effect the CMFB bandwidth?