

Design a 2-stage, open-loop, SR limited comparator (differential in, single-ended out) to meet the following specifications:

- Total propagation delay (rising or falling): $t_p \leq 60ns$
- Input common-mode range, ICMR: $0.5V \leq V_{IC} \leq 3.5V$
- Output voltage range: $V_{OH} = 4.5V$, $V_{OL} = 0.5V$
- Minimum input voltage (for full-scale output): $V_{in_min} = 1mV$
- Maximum power dissipation: $P_{diss} \leq 2.5mW$

With the following design constraints:

- Power supplies: $V_{dd} = 5V$, $V_{ss} = 0V$
- Use only one ideal current source in your final design
- Use the model files from the AMIC5 process located in (as used in 4228/5008):
 - `magellan:/usr/local/cadence/cadence/models/amic5/mos.scs` Section: typ
- Minimum device length: $L \geq 1\mu m$
- Load capacitance: $C_L = 5pF$

Turn in the following in a PowerPoint presentation file via e-mail to the instructor by the due date. Use screen-capture images from cadence for schematics and simulation results. Do not print or turn in hardcopies.

- Full schematic of your design
- Simulation results verifying that each of the above design specifications have been met