

Latched Comparator Analysis

For the latched (clocked) comparator *comp_latch* given in the *ecen5007ref* library on magellan, the objective in adding the latching transistor (M24) was to allow the outputs to swing rail-to-rail.

As the circuit is currently drawn (see *comp_latch* schematic cellview), the output swing is improved, but still only swings to a maximum of less than $(V_{dd} - 1V)$. Run transient simulations, analyze the circuit, determine why, then fix it (for rail-to-rail output). In fixing the problem, you cannot add any devices or components. Only change the wiring (node connections). Do not significantly affect the comparator operation with your fix (delay, gain, etc.).

Turn in the following (in a PowerPoint file):

- Original schematic & simulation showing poor output swing
- Explanation of why the output is limited (any combination of text, highlighted images of schematic sections, simulations, as needed)
- Schematic of the improved circuit with improvement(s) highlighted and some explanation of why you made the changes
 - Again, do not add any components or significantly alter performance
- Transient simulation showing rail-to-rail operation