

## Oscillator Design (comparators with hysteresis)

Design an on-chip oscillator using a comparator with internal hysteresis to meet the following specifications:

- Nominal output frequency: 500 kHz
- Load capacitance: 10 pF

Your design should be based on supplying alternately positive and negative current to a capacitor such that the capacitor voltage integrates up and down with near constant slope. The capacitor voltage is then input to your comparator with hysteresis to create a gating signal that switches the polarity of the current source (positive or negative), resulting in an oscillator. Design according to the following constraints:

- Select any comparator topology with internal hysteresis (e.g. Schmitt trigger, diff amp with internal feedback)
- External to your design block (in the simulation setup), you may use as many ideal current and voltage sources and devices as you need and two capacitors (one for the integration cap, one 10 pF load capacitor)
  - Note: the maximum integration capacitor size is 5 pF
- Your design block should have only nmos and pmos devices, with the following inputs and outputs:
  - vdd = 3.3V and gnd power supplies
  - two ideal voltage bias inputs (for the current sources)
  - one capacitor node (for the external oscillator capacitor)
  - one clock output

Turn in the following:

- Complete schematic of your final design
- Description of your design approach, comparator design, and design equations
- Transient simulation results demonstrating proper operation, including operation at each of the four process corners and the typical operating point. State the minimum and maximum operating frequencies.
- State the expected tolerance for the oscillator frequency given the process variations and assuming the current source and capacitor each have a tolerance of +/- 10%.
- Complete layout of your design block (not including the integration capacitor), with DRC and LVS results