

Perform the following based on your results from Archive, Problem G2:

1. Solve for the Z-transform of your 2nd-order filter from G2 part (b) using a signal flow graph approach.
2. Find a suitable solution for the following capacitor ratios in order to achieve the specifications below based on Eq (1) in archive problem G2. Use a sampling frequency of: $f_s = 1\text{MHz} = \frac{1}{T_s}$. Note that C_R is the capacitor in the SC equivalent circuit of resistor R , C_{R2} for R_2 , and C_{R3} for R_3 .

$$A_o = -1, Q = 10, \omega_o = 2\pi(50\text{kHz})$$

$$\alpha_1 = \frac{C_R}{C}, \alpha_2 = \frac{C_{R2}}{C}, \alpha_3 = \frac{C_{R3}}{C}$$

3. Use Matlab (available in undergrad labs and SIMLAB) or similar program to create a Bode plot of the frequency response of your discrete-time system from the Z-transform in (1) and the values you calculated in (2). Confirm the expected response from the gain, Q-factor, and frequency specs.
4. Perform an ideal simulation in Cadence based on the Z-transform using Verilog-A coding. Due to rounding and high Q, it is likely that your resonant frequency ($\omega_o = 2\pi f_o$) has shifted. Perform a few frequency sweeps using the parametric analysis tool to narrow in and find the frequency with gain of A_o . Use an input sinewave with 500mV amplitude.
5. What transient response do you expect at an input frequency of: $f = f_s - f_o$ (the sampling freq minus your resonant freq)? Perform a simulation to confirm your expected result.
6. Implement your SC bandpass filter using ideal amplifiers, nmos switches from the AMS library, and ideal capacitors. You can use the Verilog-A no-overlap clock generator from the course library on magellan (clk_noov in /usr/local/cadence/cadence/libraries/ecen5007ref). Select your switch and capacitor sizes to achieve less than 4mV steps worst case on the output voltage due to clock feed-through. Run simulations near 50kHz with a 500mV sinewave to verify operation.
7. Extend your design to a fully-differential version using ideal fully-differential amplifiers and an exact match of the SC feedback circuitry from the above parts for the 2nd half of the circuit. Repeat transient simulations with a differential input to verify operation, then replace the ideal amplifiers with your fully-differential amplifier from the previous assignment. You can supply an ideal voltage for the common-mode control of your amplifiers and supply an appropriate common-mode to the input voltage. Verify operation with your amplifier design in the SC band-pass filter circuit and fine tune your amplifier design as needed.

Extra Credit:

8. Perform a complete layout of the SC circuit with the nmos switches, poly-poly type capacitors, and your amplifier layout with any modifications made for this assignment.

Turn in the following:

1. Attach your solution to parts (1) & (2) to your handwritten solution to Problem G2 (signal-flow graph, z-transform, selected cap ratios).
2. Turn in simulation results to show successful completion of parts (3) to (7) and layout details if you perform the extra credit part (8). Your solution should resemble a project report, including comments detailing your approach, design, results, and conclusions.