

## 4-Bit DAC Design & Simulation

Design a simple 4-bit DAC based on binary weighted current mirrors and differential switch cells by performing the following steps.

1. Perform the design in the AMS 0.35u process (c35b4). Follow the on-line instructions for creating a directory for all designs in this process and getting started with a library.
2. First design an ideal 4-bit DAC using Verilog-A code. Also, design a Verilog-A “test-fixture” that will drive the DAC sequentially from 0 to  $2^N-1$  and automatically measure the offset & gain errors and worst-case INL and DNL (can use the ahdLib blocks “dac\_dnl\_8bit” and “dac\_inl\_8bit” as examples).
3. Verify the operation of your test fixture by adding errors into your ideal DAC and using the test fixture to measure the errors. Use  $V_{ref}=1.24V$ , clock frequency of 10MHz.
4. Look up and read the data sheet for the commercial 8-bit DAC, “dac908” from TI (Burr-Brown).
5. Design a 4-bit current-steering DAC to match the functional operation of the “dac908”, based on the following constraints and assumptions:
  - a. Assume external 1.24V reference (no need for INT/EXT circuitry)
  - b. Do not include latches or power-down (PD)
  - c. Only analog supplies,  $V_a = 3.3V$ ,  $AGND=0V$
  - d. Create a symbol for your design with the following pins:  $V_A$ ,  $BW$ ,  $I_{out}$ ,  $I_{out\_bar}$ ,  $D3..D0$ ,  $CLK$ ,  $AGND$ ,  $REF_{IN}$ ,  $FSA$
  - e. Use an external resistor to set the reference current to 20uA with  $V_{ref}=1.24V$
  - f. Design for ideal outputs:
 
$$I_{out} = 4 \cdot I_{REF} \left( \frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16} \right), \quad I_{out\_bar} = \left( 4 - \frac{1}{4} \right) I_{ref} - I_{out}$$
  - g. You have available one ideal amplifier (Verilog-A) and as many n & p type transistors as you need (bias and output resistors are external to the chip)
6. Create a test schematic that includes:
  - a. 4-bit DAC and “test-fixture”
  - b.  $V_a=3.3V$  and  $V_{ref}=REF_{IN}=1.24V$  power supplies & a clock
  - c. DAC bias resistor for  $I_{ref}=20uA$
  - d. Load both outputs with matched resistors to achieve differential output voltages between 0V and (1.24V-LSB)
7. Run a transient simulation to allow your test-fixture to sweep through the 16 digital inputs at a clock rate of 10MHz & record the offset, gain, INL and DNL errors.
8. Make any adjustments necessary to achieve INL & DNL errors  $< +/- 0.5LSB$
9. What is the maximum conversion frequency of your DAC (to settle within 0.5LSB)?
10. Bullet at least 3 options for improving the performance of your DAC (resolution and/or speed).

Turn in (e-mail) a PowerPoint presentation verifying that you have succeeded in each of the above tasks.