

4-Bit ADC Design & Simulation

Design a 4-bit successive approximation ADC based on your DAC from Problem H1 by performing the following steps.

1. Again, design in the AMS 0.35u process (c35b4).
2. Design a successive approximation register (SAR) for your ADC using Verilog coding (or VHDL if you prefer). Verify your code using a digital simulator (Verilog-XL in Cadence on magellan or other tools if you prefer) and stimulus or test-bench code (show results in your ppt solution).
 - a. Note, to run Verilog-XL: *magellan> verilog +gui -s <file.v>*
3. Create and test a functional schematic of your complete 4-bit ADC, including:
 - a. SAR: create “functional” verilog view, Cadence will create symbol
 - b. Comparator: use ideal veriloga code
 - c. DAC: use either ideal veriloga or your already tested and working DAC from H1 (use a single-ended version of H1 → only one DAC output, not differential)
 - d. Other peripheral test components (clock, power supply, reference, etc.)
 - e. Run mixed-signal simulation using “spectreVerilog” simulator.
 - f. Run the ADC with a clock rate of 1MHz with a constant input voltage (sample rate of 250kHz), $V_{ref}=1.24V$, $V_{dd}=3.3V$.
4. Implement the amplifier in your DAC and the ADC comparator with the following constraints:
 - a. You can use one ideal current source (for both DAC amp and comparator)
 - b. Otherwise, use only nmos4 and pmos4 devices from the “PRIMLIB” library
 - c. Independently verify each amplifier (outside of ADC/DAC sims) to show they will meet the requirements of the ADC system.
5. Put it all together and verify complete ADC operation
 - a. All components at the transistor level except:
 - i. SAR in verilog
 - ii. one ideal i-source for amps
 - iii. two external resistors for DAC reference and output load
 - iv. Vdd power supply, Vref and Vin, clock.
 - b. Show operation at five input voltages, 0V, $0.25*V_{ref}$, $0.5*V_{ref}$, $0.75*V_{ref}$, V_{ref} .

Turn in (e-mail) a PowerPoint presentation verifying you have succeeded in each of the above tasks.