

Buffer design (exercise in Cadence software tools): Design a logic buffer using two cascaded inverters with width over length ratios of:

- Inverter 1: $(W/L)_{n1} = 1 / 0.35\mu$, $(W/L)_{p1} = 3 / 0.35\mu$
- Inverter 2: $(W/L)_{n2} = 3 / 0.35\mu$, $(W/L)_{p2} = 9 / 0.35\mu$

Design and simulation: complete the following steps

- Create schematic, symbol and layout views for each inverter separately, including Assura DRC and LVS verification
 - For DRC, use the no_coverage and no_generated_layers switches
- Create a top level schematic, symbol and layout for the complete buffer by placing the two inverters into a new cell, including Assura DRC and LVS verification
- Note: for the IC schematics above, place A4 borders around the devices from the BORDERS library (do not use a border for the simulation schematic below)
- Create a simulation schematic for the buffer and perform the following transient:
 - Power supply, Vdd = 3.3V
 - Input signal: 0 to 3.3V, 1MHz square wave input with 5ns rise and fall times
 - No load
- Extract the final layout with Assura RCX tool
- Simulate the schematic and extracted versions of the design together
 - Generate a config view of the buffer simulation schematic and place two cells of the complete buffer in the schematic
 - Assign one cell to simulate as view 'schematic'
 - Assign the other cell to simulate as view 'av_extracted'
 - Compare the results

Turn in the following:

- Complete set of schematics (final simulation setup, buffer and individual inverters)
- Layout of complete buffer
- The last ~8 lines of the LVS log file, including:
 - Top cell ...
 - Schematic and Layout match ...
 - ...
 - Run ended ...
- Simulation plots showing
 - 3us of simulation transient with input and schematic and extracted outputs
 - Zoom in of the same on falling transition of outputs showing difference between schematic and extracted results