

Clock generator design: Design an on-chip clock generator to meet the following specifications:

- Clock frequency: **500 kHz (nominal)**
- Duty cycle: **50 %**
- Cell I/O: No inputs, only one output: **clock**
 - Top cell symbol view should be a block with one output and requires only global signal **vdd!** to be defined for proper simulation

Procedure: complete the following steps

- Create a top level schematic of the clock generator. Include the following four components. For the first two blocks, use the Add → Block... (shortcut 'b') to create symbols (despite having no other views yet)
 - Comparator with hysteresis
 - Current control block (to source & sink current)
 - Charging capacitor (poly1-poly2 cap: 'cpoly' in PRIMLIB)
 - Output buffer (use result from HW #1)
 - Wire the four components together. This will auto-create pins on the first two blocks when wires are connected to the block. Re-name the pins and pin types as appropriate.
- Create 'veriloga' views of the hysteresis comparator and current control blocks
 - Examples are available on the course library on magellan
- Verify the functional design
 - Adjust parameters for hysteresis, current control and capacitor size to meet the specifications
 - Verify design by simulation
 - **NOTE: to avoid issues with a dc solution, go to the simulator Analyses → tran → Options... → skipdc: check yes**
- Complete transistor level design (use pcells for layouts as desired)
 - Implement the comparator using a Schmitt trigger followed by an inverter (use any inverter from CORELIB or HW#1)
 - Complete a schematic view, verify by simulation, complete layout (DRC & LVS)
 - Implement the current control block
 - For the resistor, use high resistance poly ('rpolyh' in PRIMLIB)
 - Complete a schematic view, verify by simulation, complete layout (DRC & LVS)
- Full design simulation
 - Verify full operation under nominal conditions
 - Perform Corners simulation with worst case values for the resistor and capacitor, but typical for transistors. Record the range of frequencies.
 - Extra credit: Perform a Monte Carlo statistical simulation
 - Use 100 simulation points, process and matching variations
 - Use the calculator to set an expression for automatically calculating the frequency
 - Plot a Histogram of the resulting frequency variation

Turn in:

- Full set of schematics (top level, sub-blocks, **not** including any re-use from HW#1)
- Top level layout (complete clock generator), with results showing clean LVS & DRC
- Simulation results
 - Waveform from functional design
 - Waveforms from complete design, with tabulated results on frequency from corner analysis
 - Extra credit: histogram from Monte Carlo simulation on frequency variation