

**Differential comparator:**

Design a 2-stage, open-loop, SR limited comparator (differential in, single-ended out) to meet the following specifications:

- Total propagation delay (rising or falling):  $t_p \leq 100ns$  with  $1pF$  load capacitance
- Input common-mode range, ICMR:  $0.5V \leq V_{IC} \leq 1.5V$
- Approx. rail-to-rail output stage
- Minimum input voltage (for full-scale output):  $V_{in\_min} = 2.5mV$
- Maximum quiescent power dissipation:  $P_{diss} \leq 200\mu W$

With the following design constraints:

- Power supplies:  $V_{dd} = 3.3V$ ,  $V_{ss} = 0V$
- Use one resistor and as many nmos and pmos devices as needed in the design (note: the load capacitance is external to the design, not in cell schematic or layout).
- Load capacitance:  $C_L = 1pF$

**Turn in:**

- Comparator schematic and layout (including bias resistor and all devices), with results showing clean LVS & DRC
- Simulation results
  - Appropriate waveforms demonstrating that each of the specifications are met under nominal conditions
  - Histogram plot from Monte Carlo simulation on propagation delay with 30 simulation runs. Note the mean and standard deviation for the delay. NOTE: use an ideal load capacitor from the analogLib in your simulation schematic so there are no load variations in the simulation.