

Latched differential comparator with hysteresis:

Design a latched comparator with hysteresis to meet the following specifications and perform the testing and additional design as described below.

- Valid operation with a clock frequency of 25 MHz
- Input common-mode range, ICMR: $0.5V \leq V_{IC} \leq 1.5V$
- Approx. 100mV of hysteresis
- Approx. rail-to-rail output stage

With the following design constraints:

- Power supplies: $V_{dd} = 3.3V$, $V_{ss} = 0V$
- Use one resistor and as many nmos and pmos devices as needed in the design
- Load capacitance: negligible

Procedure

- Design the comparator and verify correct ICMR and hysteresis while in the track mode (no clock signal). Verify hysteresis with a 1V DC signal on the minus input and a triangle waveform on the plus input (0.5V to 1.5V, 2us rise and 2us fall times).
- Verify latch operation with a 25MHz, 3.3V, 50% duty cycle clock signal and the same triangle wave on the input described above.
- Create a new schematic with the latched comparator followed by a D-type flip-flop (FF) from the CORELIB library (connected to the plus comparator output). Add an inverter if needed (from CORELIB or past homework) so the clock signal drives the comparator in the latch mode when low, track mode when high, and triggers the FF on the rising edge. Perform analog simulations (no config view is needed).
- Verify the comparator with flip-flop, again with the same triangle wave input. Verify the FF output transitions only once near each trip point of the input voltage as expected.
- Add a sinusoidal source in series with the triangle wave input to emulate high frequency noise on the input signal. Use a source with 25mV amplitude, 100MHz frequency, zero DC. Verify again that the FF output only triggers once at each expected input trip point (is not sensitive to the input noise).

Turn in:

- Comparator schematic and layout (including bias resistor and all devices), with results showing DRC & LVS clean
- Complete schematic and layout including the comparator, flip-flop and any inverters, show DRC & LVS clean
- Simulation results
 - Verification of ICMR
 - Plots from transient simulations with triangle wave input, including:
 - Track operation only (no clock signal); Label hysteresis trip points on the input waveform (at input voltage where the plus and minus outputs cross)
 - Latch operation with 25MHz clock, no FF
 - Latch operation with clock and FF
 - Latch operation with clock and 100MHz “noise” on triangle wave input