

3-Bit Charge Scaling DAC

Design a 3-bit charge scaling DAC based on the “serial charge redistribution” approach (e.g. using two capacitors, three switches and digital control logic). Meet the following specifications:

- Maximum conversion time: $T_{c_max} = 200$ ns
- Output voltage settled to within 0.5 LSB of the ideal output:

$$V_o = \left(\frac{b_2}{2} + \frac{b_1}{4} + \frac{b_0}{8} \right) \cdot 1V$$

- No output buffer is required. The output only needs to be valid at the end of the last clock period in the conversion cycle.
- Assume there is an unknown load capacitance of up to, $C_{L_max} = 500$ fF
- I/O: binary input word: $[b_2 \ b_1 \ b_0]$, input reference V_{ref} , input clock clk , input $reset$, output voltage, V_o , and power supplies.

With the following design constraints:

- Power supplies: $V_{dd} = 3.3V$, $V_{ss} = 0V$
- Use an ideal reference supply for simulations, $V_{ref} = 1.0V$
- Use an ideal clock input, clk , with a frequency of your choosing (to meet T_{c_max} limit)
- Use two poly type capacitors for the charge-scaling
- Use as many nmos and pmos devices as desired (don't go crazy, just need three switches)

Procedure

- Design the analog section (caps & switches) to meet the specifications
- Follow the online tutorials for automated synthesis, place & route and verification
- Write Verilog code for dac controller. Example code (requiring minor editing) can be downloaded from
 - `/usr/local/cadence/cadence/homework/dac_control_hw.v`
- Verify your design using mixed-signal simulation with the ideal Verilog code and a modified DAC test fixture
- Perform synthesis, place & route, import and LVS for the control block
- Complete the full DAC layout with LVS
- Test the complete design via pure analog simulation with the test fixture

Turn in

- Top level schematic, final code for control and test fixture blocks and top level layout with results showing LVS clean.
- Mixed-signal (ideal control) and full analog transient response with 100ns conversion time steps, sequencing through all inputs from 0 to 7, showing the output voltage and thermometer code drive signals
- Text output from test fixture output file, showing offset and gain errors, data from each input, and INL and DNL errors.
- **Extra credit:** Assuming the charge scaling capacitors are identical, $C_1 = C_2$, find a general expression for the minimum allowed ratio between the charge capacitors and load capacitor, C_1/C_L , for an N bit version of the DAC (worst case +/- 0.5LSB error). Solve this ratio for N = 3 and 8. Assume the DAC is designed neglecting C_L and there are no other errors in the circuit.